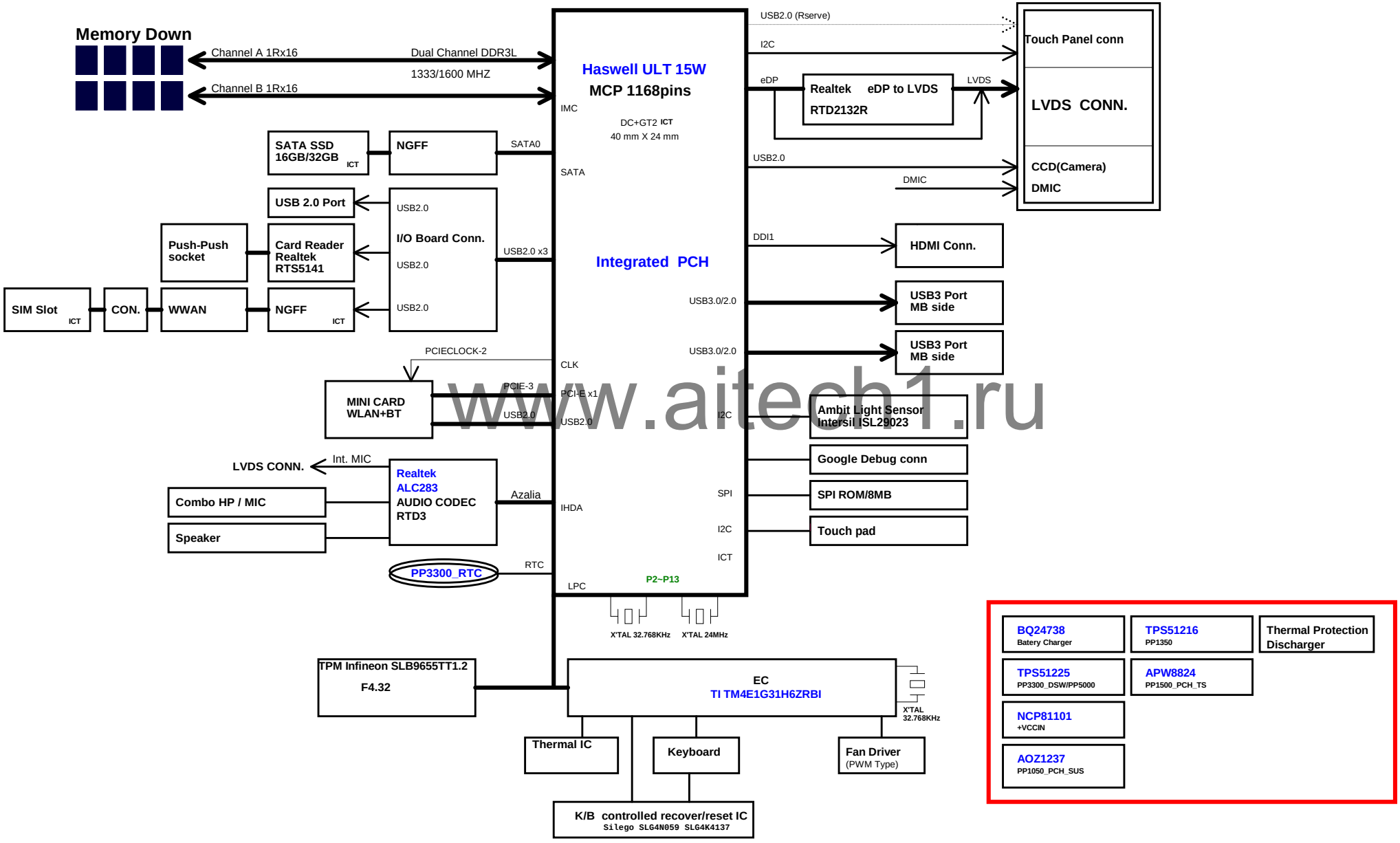
# A23 SHB ULT SYSTEM BLOCK DIAGRAM




| | | |
|---|---|---|
| BQ24738<br>Batery Charger | TPS51216<br>PP1350 | Thermal Protection<br>Discharger |
| TPS51225<br>PP3300_DSW/PP5000 | APW8824<br>PP1500_PCH_TS | |
| NCP81101<br>+VCCIN | | |
| AOZ1237<br>PP1050_PCH_SUS | | |



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|---|---|---|---|
| C | Block Diagram | ICT | 1A |
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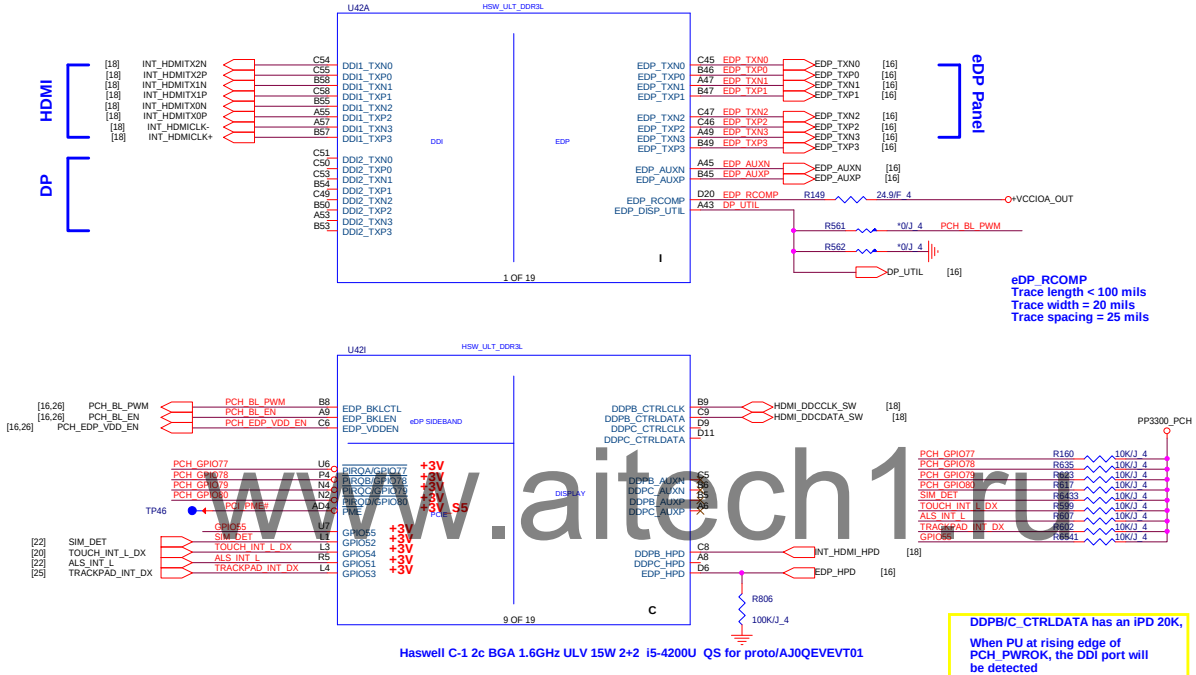
# Haswell ULT (DISPLAY,eDP)




Haswell C-1 2c BGA 1.6GHz ULV 15W 2+2 i5-4200U QS for proto/AJ0QEVEVT01



| | | | |
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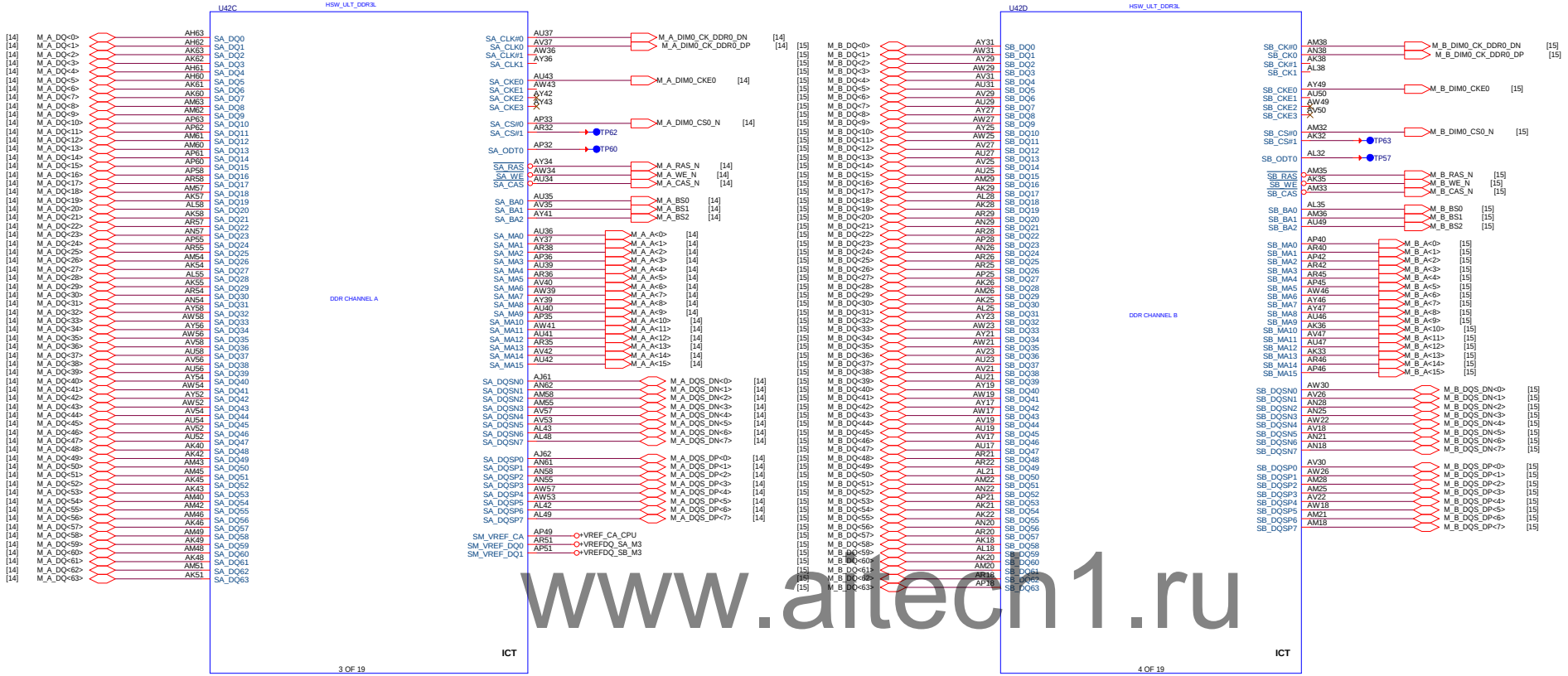
# Haswell ULT (DDR3L)

# Haswell Processor (DDR3L)








| | |
|---|---|
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| Rev: 1A | |
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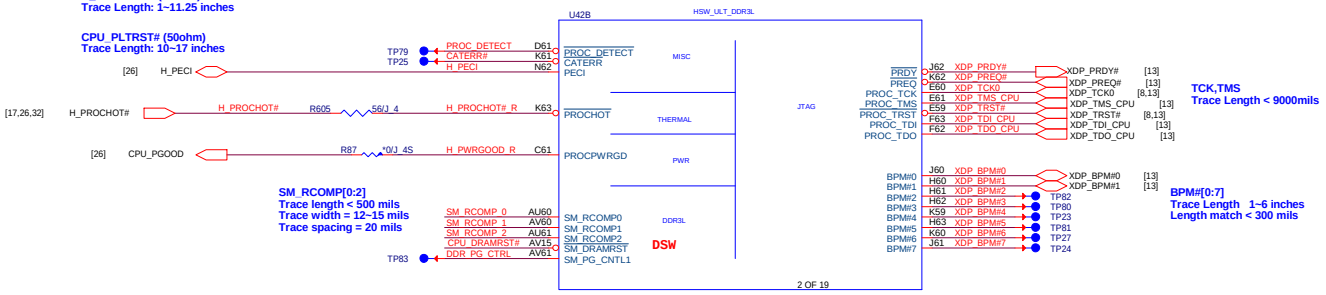
# Haswell ULT (SIDEBAND)

**H_PECI (50ohm)**
**Route on microstrip only**
**Spacing >18 mils**
**Trace Length: 0.4~6.125 iches**

**H_PWRGOOD (50ohm)**
**Trace Length: 1~11.25 inches**

**CPU_PLTRST# (50ohm)**
**Trace Length: 10~17 inches**



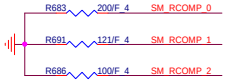

**TCK,TMS**
**Trace Length < 9000mils**

**SM_RCOMP[0:2]**
**Trace length < 500 mils**
**Trace width = 12~15 mils**
**Trace spacing = 20 mils**

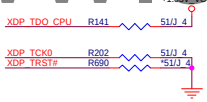
**BPM#[0:7]**
**Trace Length 1~6 inches**
**Length match < 300 mils**



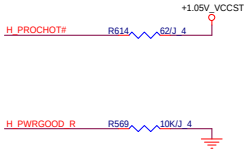
## DRAM COMP



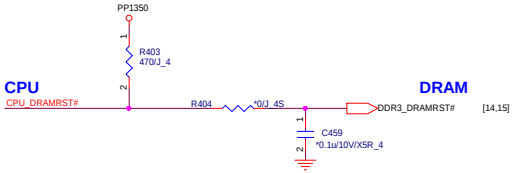

## XDP PU/PD




## PU/PD of CPU




## DRAMRST




[5,10] [5,14,15,30] +1.05V_VCCST PP1350 → +1.05V_VCCST PP1350 → +1.35V_SUS

| | | | |
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# Haswell ULT (POWER)

| VDDQ Output Decoupling Recommendations | | |
|---|---|---|
| 330uFx2 | 7343 | BOT socket side |
| 22uFx11 | 0805 | 5 onTOP, 6 on BOT inside socket cavity |
| 10uFx10 | 0805 | 5 onTOP, 5 on BOT inside socket cavity |

| VCC Output Decoupling Recommendations | | |
|---|---|---|
| 470uFx4 | 7343 | TOP socket side |
| 22uFx8 | 0805 | 4 on TOP, 4 on BOT near socket edge |
| 22uFx11 | 0805 | TOP, inside socket cavity |
| 10uFx11 | 0805 | BOT, inside socket cavity |

## VCCST PWRGD

[13,26,31] PP1050_PGOOD — R579 *0/J_4
[7,26] PCH_PWROK — R544 *0/J_4S
[7,13,26] SYS_PWROK — R580 *0/J_4

U38 74AUP1G07GW (ICT): NC, VCC, A, GND, Y

PP3300_DSW — C584 0.1U/10V/X5R_4

CRB is via +1.05V PG

+1.05V_VCCST — R551 10K/J_4

R545 *0/J_4S — C582 *0.1u/10V/X5R_4

Reserve: D46 *RB501V-40

VCCST_PWRGD_EN — VCCST_PWRGD_R

0415 VCCST PWRGD

G Path

[13] VCCST_PWRGD — [32] VRON_CPU — [10,32] VCORE_PGOOD

0415 VCCST PWRGD need PP1050_RUN power good

[13] PWR_DEBUG — R173 *0/J_4S — PWR_DEBUG_R

+1.05V_VCCST — R566 *10K/J_4 — R567 =10K/J_4 — R151 150/J_6

## Layout note: need routing together and ALERT need between CLK and DATA.

### SVID

Place PU resistor close to CPU

+1.05V_VCCST — R618 130/F_4

[32] VR_SVID_DATA — R625 *0/J_4S — H_CPU_SVIDDAT

Place PU resistor close to CPU

+1.05V_VCCST — R640 75/J_4

[32] VR_SVID_ALERT# — R630 43/J_4 — H_CPU_SVIDART#

+1.05V_VCCST — R6554 54.9/F_4 — C5667 0.1U/10V/X7R_4

[32] VR_SVID_CLK — R641 *0/J_4S — H_CPU_SVIDCLK

PP1350

C5658 10u/6.3V/X5R_6 — C5657 10u/6.3V/X5R_6 — C5656 10u/6.3V/X5R_6 — C5660 2.2u/6.3V/X7R_6 — C5659 2.2u/6.3V/X7R_6

+1.35V_CPU 1.4A

C225 22u/6.3V/X5R_8 — C261 10u/6.3V/X5R_6 — C260 10u/6.3V/X5R_6 — C259 10u/6.3V/X5R_6 — C224 2.2u/6.3V/X7R_6 — C256 2.2u/6.3V/X7R_6

+VCCIN — R583 100/F_4 — [32] VCC_SENSE — R587 *0/J_4S

300mA

+VCCIOA_OUT

300mA

+VCCIN — EC14 *1U/6.3V/X5R_4 — EC15 *470p/50V/X7R_4

Reserve for RF

PP1050_PCH — R190 *0/J_8S — +1.05V_VCCST

C223 *4.7u/6.3V/X5R_6

+VCCIN

U42L — HSW_ULT_DDR3L

| | | |
|---|---|---|
| TP29 | ULT_RVSD_61 | L59 RSVD |
| TP20 | ULT_RVSD_62 | J58 RSVD |
| | | AH26, AJ31, AJ33, AJ37, AN33, AP43, AR48, AY35, AY40, AY44, AY50 VDDQ |
| | | F59 VCC |
| TP28 | ULT_RVSD_63 | N58 RSVD |
| TP41 | ULT_RVSD_64 | AC58 RSVD |
| | VCC_SENSE_R | E63 VCC_SENSE |
| TP42 | ULT_RVSD_65 | AB23 RSVD |
| TP514 | +VCCIO_OUT | A59 VCCIO_OUT |
| | | E20 VCCIOA_OUT |
| TP43 | ULT_RVSD_66 | AD23 RSVD |
| TP47 | ULT_RVSD_67 | AA23 RSVD |
| TP50 | ULT_RVSD_68 | AE59 RSVD |
| | H_CPU_SVIDART# | L62 VIDALERT |
| | H_CPU_SVIDCLK | N63 VIDSCLK |
| | H_CPU_SVIDDAT | L63 VIDSOUT |
| | VCCST_PWRGD | B59 VCCST_PWRGD |
| | VRON_CPU | F60 VR_EN |
| | VCORE_PGOOD | C59 VR_READY |
| | PWR_DEBUG_R | D63 VSS |
| | | H59 PWR_DEBUG |
| | | P62 VSS |
| TP30 | ULT_RVSD_69 | P60 RSVD_TP |
| TP31 | ULT_RVSD_70 | P61 RSVD_TP |
| TP26 | ULT_RVSD_71 | N59 RSVD_TP |
| TP85 | ULT_RVSD_72 | N61 RSVD_TP |
| TP32 | ULT_RVSD_73 | T59 RSVD_TP |
| TP49 | ULT_RVSD_74 | AD60 RSVD |
| TP51 | ULT_RVSD_75 | AD59 RSVD |
| TP36 | ULT_RVSD_76 | AA59 RSVD |
| TP39 | ULT_RVSD_77 | AE60 RSVD |
| TP37 | ULT_RVSD_78 | AC59 RSVD |
| TP54 | ULT_RVSD_79 | AG58 RSVD |
| TP35 | ULT_RVSD_80 | U59 RSVD |
| TP34 | ULT_RVSD_81 | V59 RSVD |
| | | AC22, AE22, AE23 VCCST |
| | | AB57, AD57, AG57, C24, C28, C32 VCC |

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HSW ULT POWER

ICT

+VCCIN 32A

C190 22u/6.3V/X5R_8 — C46 22u/6.3V/X5R_8 — C73 22u/6.3V/X5R_8 — C228 22u/6.3V/X5R_8 — C75 *22u/6.3V/X5R_8

C210 22u/6.3V/X5R_8 — C567 *22u/6.3V/X5R_8 — C557 22u/6.3V/X5R_8 — C201 22u/6.3V/X5R_8 — C206 22u/6.3V/X5R_8 — C202 22u/6.3V/X5R_8

C562 22u/6.3V/X5R_8 — C167 22u/6.3V/X5R_8 — C45 22u/6.3V/X5R_8 — C169 22u/6.3V/X5R_8 — C165 22u/6.3V/X5R_8 — C171 22u/6.3V/X5R_8

C204 22u/6.3V/X5R_8 — C173 22u/6.3V/X5R_8 — C172 22u/6.3V/X5R_8 — C170 22u/6.3V/X5R_8 — C203 22u/6.3V/X5R_8 — C205 22u/6.3V/X5R_8

C168 22u/6.3V/X5R_8 — C71 22u/6.3V/X5R_8 — C74 22u/6.3V/X5R_8

| | | |
|---|---|---|
| [2] | +VCCIOA_OUT | +VCCIOA_OUT |
| [32] | +VCCIN | +VCCIN |
| [4,10] | +1.05V_VCCST | +1.05V_VCCST |
| [4,14,15,30] | PP1350 | PP1350 |
| [11,13,26,31] | PP1050_PCH | PP1050_PCH |
| [7,8,10,11,13,20,21,24,25,26,28,29,33] | PP3300_DSW | PP3300_DSW |



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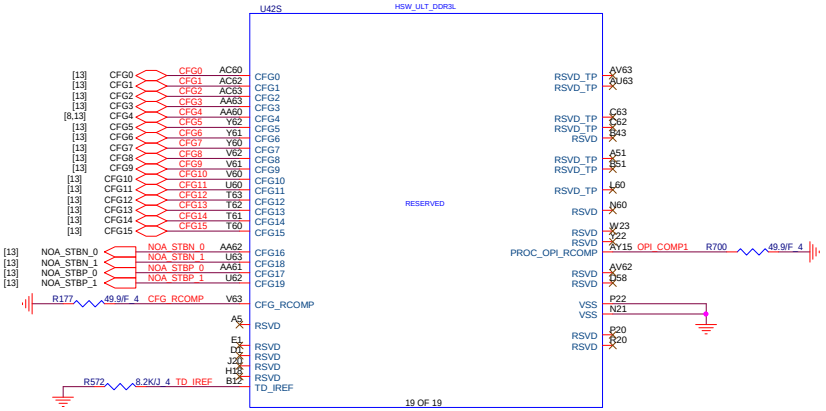
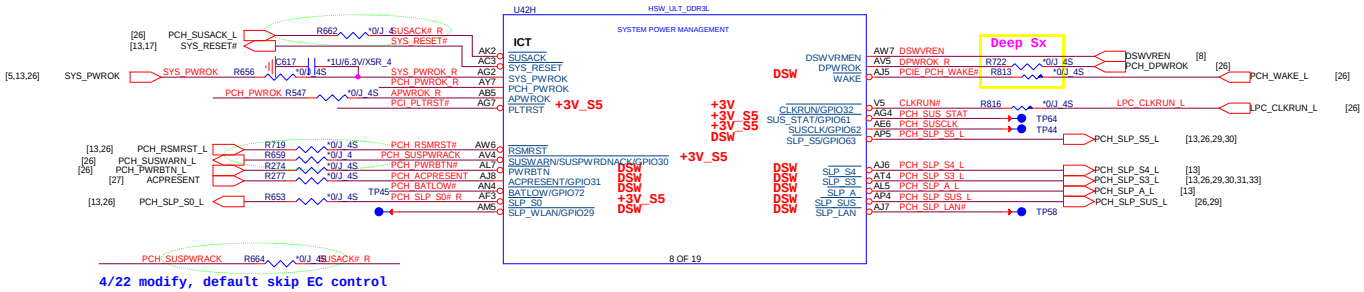
# Haswell ULT (CFG,RSVD)

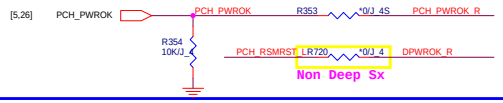



## Processor Strapping

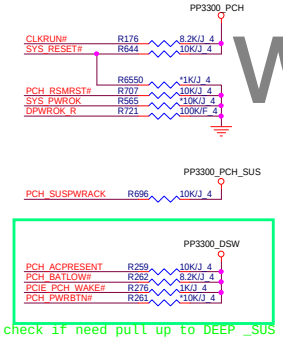
| | 1 | 0 | |
|---|---|---|---|
| CFG0<br>EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED | (DEFAULT) NORMAL OPERATION; NO STALL | STALL | CFG0 R203 *1K/J_4 |
| CFG1<br>PCH/ PCH LESS MODE SELECTION | (DEFAULT) NORMAL OPERATION | PCH-LESS MODE | CFG1 R184 *1K/J_4 |
| CFG3<br>PHYSICAL_DEBUG_ENABLED (DFX PRIVACY) | DISABLED<br>NO PHYSICAL DISPLAY PORT ATTACHED TO<br>EMBEDDED DISPLAY PORT | ENABLED<br>AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED<br>TO THE EMBEDDED DISPLAY PORT | CFG3 R192 *1K/J_4 |
| CFG 8<br>ALLOW THE USE OF NOA ON LOCKED UNITS | DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS | ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT | CFG8 R171 *1K/J_4 |
| CFG9<br>NO SVID PROTOCOL CAPABLE VR CONNECTED | VRS SUPPORTING SVID PROTOCOL ARE PRESENT | NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY | CFG9 R172 *1K/J_4 |
| CFG10<br>SAFE MODE BOOT | POWER FEATURES ACTIVATED DURING RESET | POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED | CFG10 R183 *1K/J_4 |
| | | | |

# Haswell ULT PCH (PM)

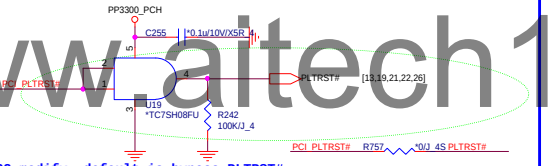


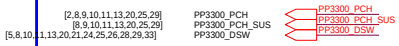




## PCH PM PU/PD




## PLTRST# Buffer






| | | | |
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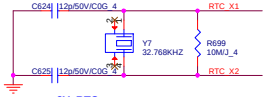
# Haswell ULT PCH (RTC/HDA/SATA/SPI)

# Haswell ULT PCH(LPC,SPI,SMBUS,C-LINK,THERMAL)

# 08

## RTC Clock 32.768KHz (RTC)

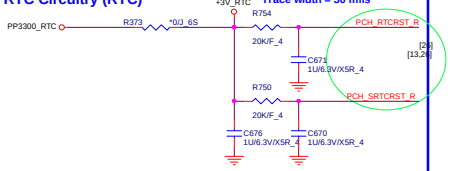



+3V_RTC
Trace width = 20 mils

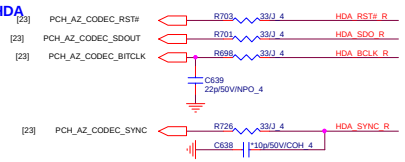
## RTC Circuitry (RTC)

+3V_RTC
Trace width = 30 mils

check if need connect to PCH_RTCRST_R/PCH_SRTCRST_R



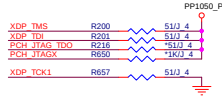

## HDA




## PCH JTAG

JTAG_TCK,JTAG_TMS
Trace Length < 9000mils

MP remove(Intel)



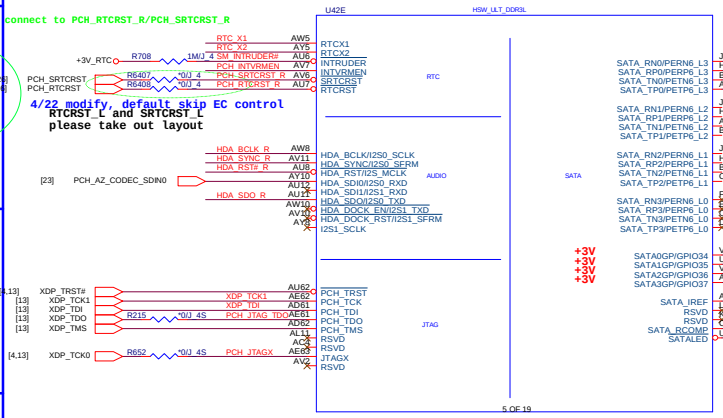

## ULT Strapping Table

| Pin Name | Strap description | Sampled | Configuration | note |
|---|---|---|---|---|
| GPIO81(SPKR) | No reboot on TCO Timer expiration | PWROK | 0 = Default enable (iPD 20K)<br>1 =Disable No-Reboot mode | |
| HDA_SDO | Flash Descriptor Security Override / Intel ME Debug Mode | PWROK | 0 = Default can program ME (iPD 20K)<br>1 =can't program ME | |
| INTVRMEN | Integrated 1.05V VRM enable | ALWAYS | 1=Should be always pull-up | |
| GPIO66 | Top-Block Swap override | | 0 = Default disable (iPD 20K)<br>1 = Enable TBS function | |
| GPIO86 | Boot BIOS Strap Bit | | 0 = Default SPI (iPD 20K)<br>1 =LPC | |
| GPIO15 | TLS(Transport layer security) | | 0 = Default enable w/o confidentiality(iPD 20K)<br>1 =Default enable with confidentiality | |
| CFG4 | DP presence strap | | 0 = Enable an external display port is connected to the eDP<br>1 =disable | |
| DSWVREN | Deep Sx well on die VR enable | | 1=Should be always pull-up | |

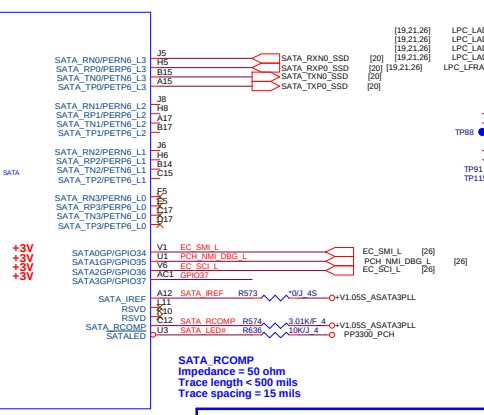


## U42E (HSW_ULT_DDR3L)

4/22 modify, default skip EC control
RTCRST_L and SRTCRST_L
please take out layout

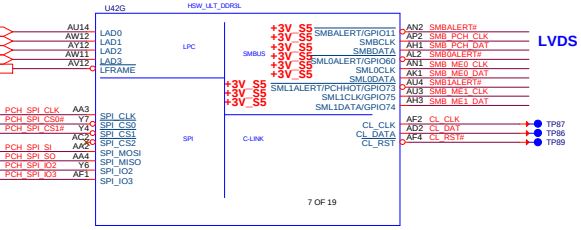



## SATA




SATA_RCOMP
Impedance = 50 ohm
Trace length < 500 mils
Trace spacing = 15 mils

## U42G (HSW_ULT_DDR3L)

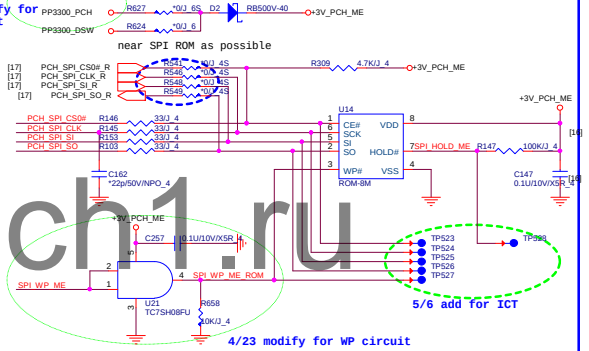



LVDS Bridge

## PCH dual I/O SPI ROM

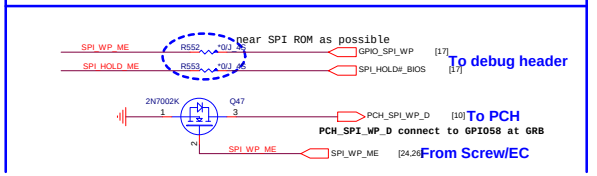
W25Q64FVSSIG(SOIC) / AKE3EFP0N06----->8MB

4/23 modify for WP circuit

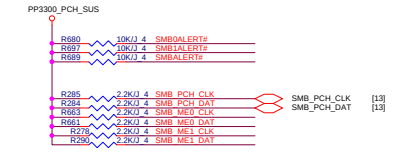


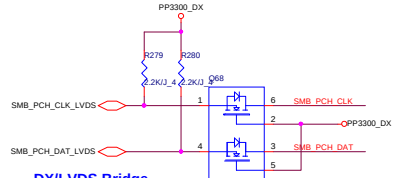

5/6 add for ICT

4/23 modify for WP circuit



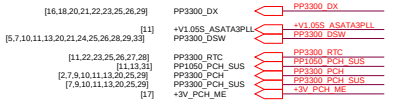

## SMBus




DX/LVDS Bridge

PCH_SUS/PCH

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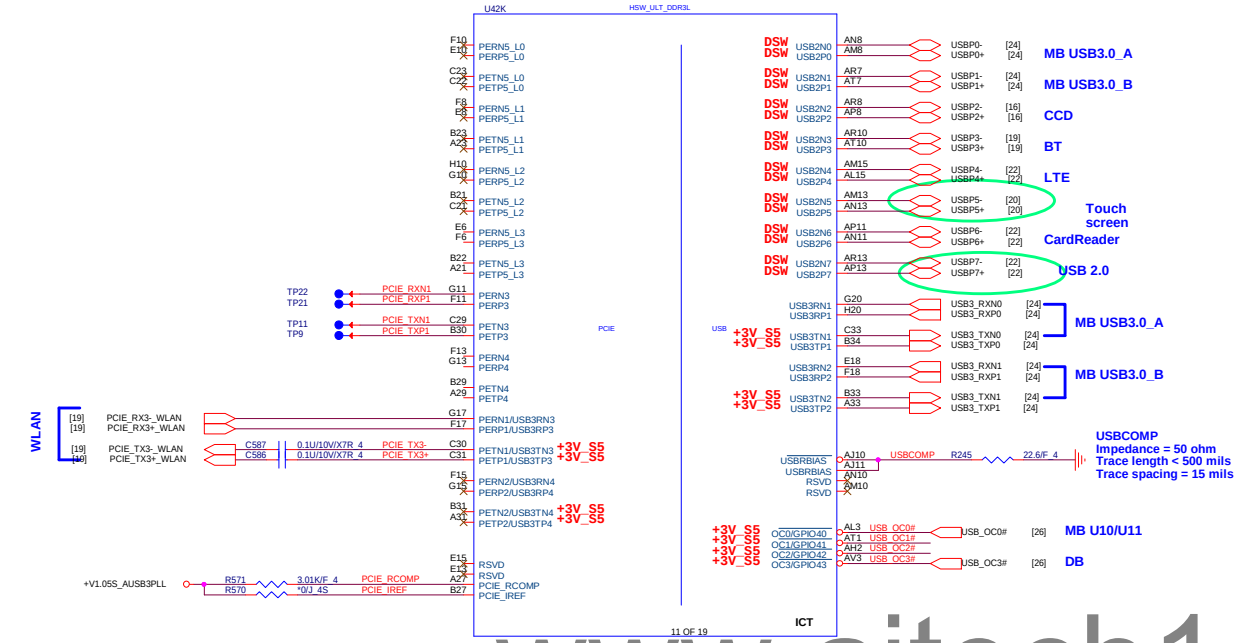
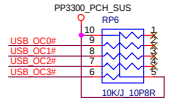
# Haswell ULT PCH (PCIE,USB3.0,USB2.0)

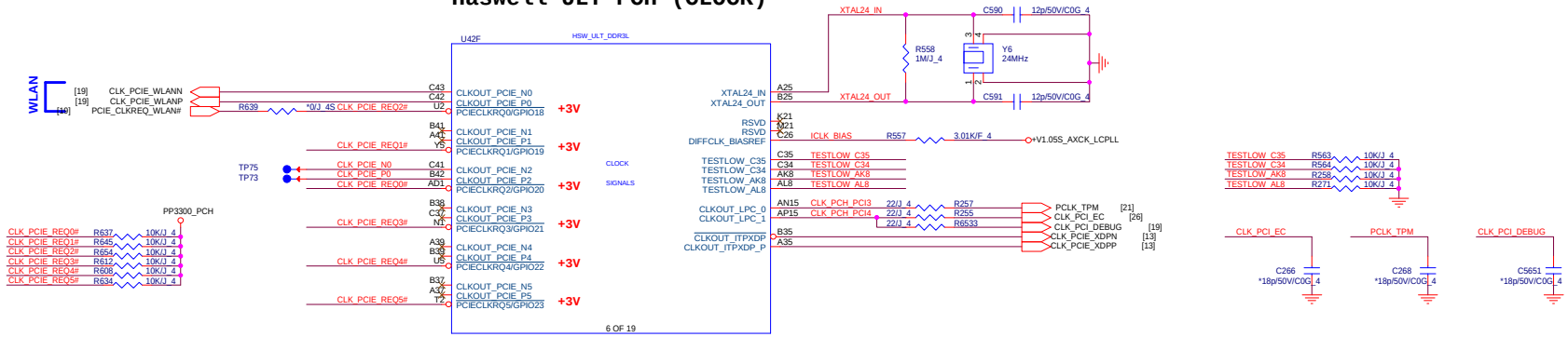



## USB Overcurrent






# Haswell ULT PCH (CLOCK)







[11] +V1.05S_AUSB3PLL → +V1.05S_AUSB3PLL

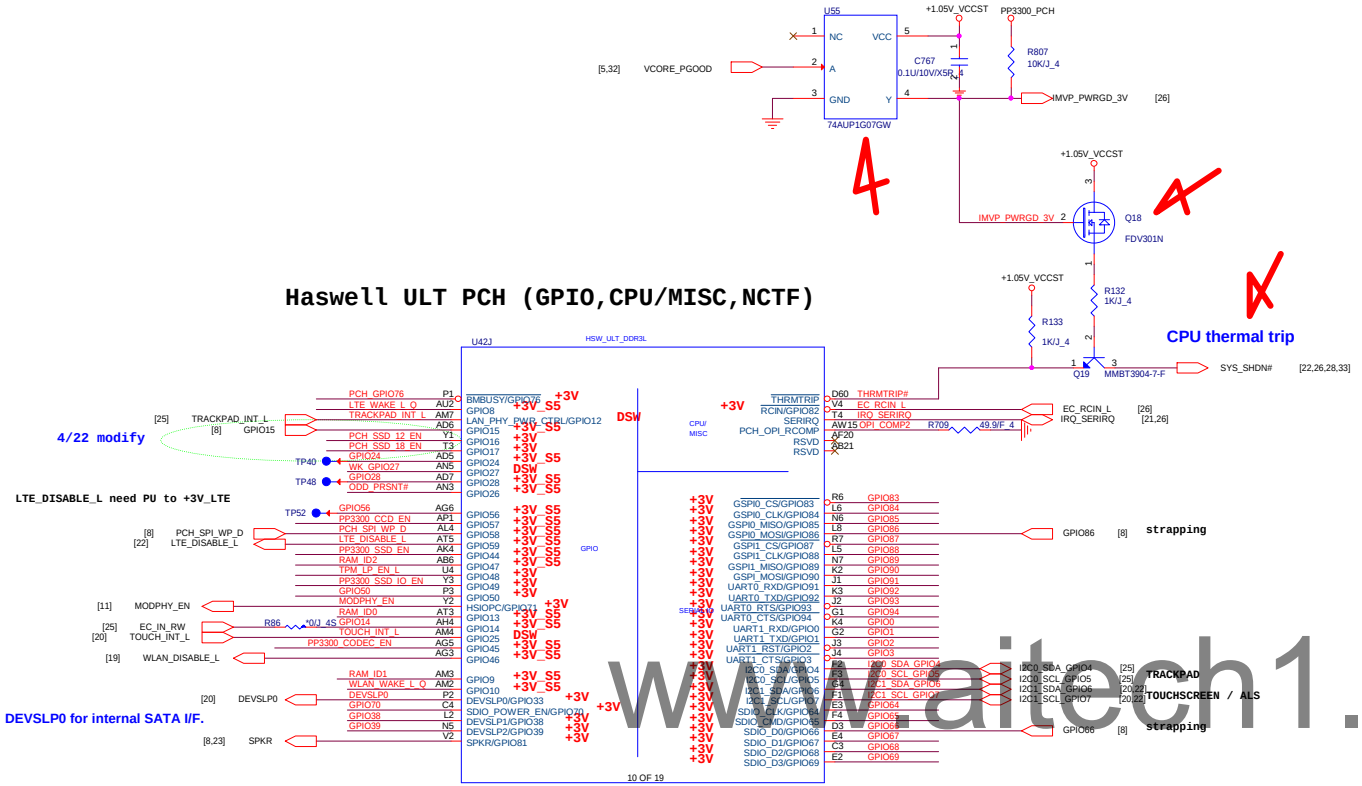
[7,8,10,11,13,20,25,29] PP3300_PCH_SUS → PP3300_PCH_SUS

[2,7,8,10,11,13,20,25,29] PP3300_PCH → PP3300_PCH

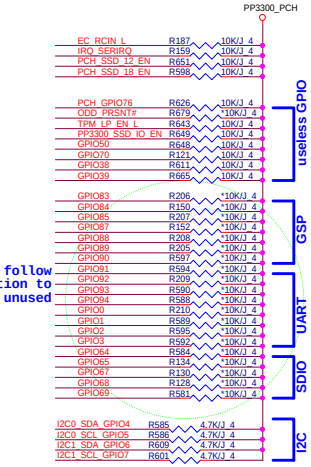
[11] +V1.05S_AXCK_LCPLL → +V1.05S_AXCK_LCPLL

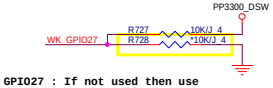
| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : A23 | | |
| Size: C | Document Number: PCH 3/6 (PCIE/USB/CLK) | Rev: 1A |
| Date: Tuesday, August 20, 2013 | Sheet: 9 of 42 | |

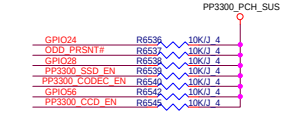
# Haswell ULT PCH (GPIO,CPU/MISC,NCTF)

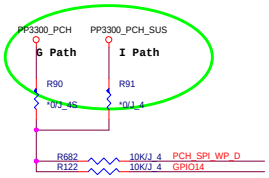


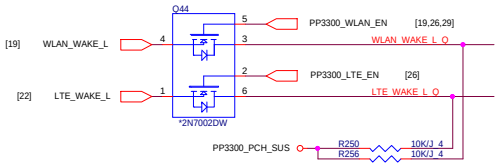

## PCH GPIO PU/PD

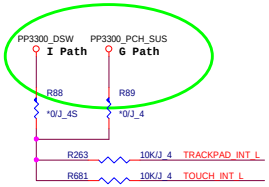


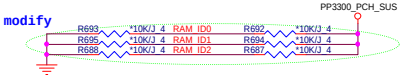




## RAM ID

4/22 modify




| Vender | Part Number | Size/Chip (Bit) | Install Quantity | Total size (Bytes) | RAM_ID2/RAM_ID1/RAM_ID0 |
|---|---|---|---|---|---|
| Micron | MT41K256M16HA-125:E | 4G | 8 | 4G | 000 |
| Hynix | H5TC4G63AFR-PBA | 4G | 8 | 4G | 001 |
| Elpida | EDJ4216EFBG-GN-F | 4G | 8 | 4G | 010 |
| Micron | MT41K256M16HA-125:E | 4G | 4 | 2G | 011 |
| Hynix | H5TC4G63AFR-PBA | 4G | 4 | 2G | 100 |
| Elpida | EDJ4216EFBG-GN-F | 4G | 4 | 2G | 101 |
| | | | | | |
| | | | | | |

[7,8,9,11,13,20,25,29] PP3300_PCH_SUS → PP3300_PCH_SUS
[4,5] +1.05V_VCCST → +1.05V_VCCST
[2,7,8,9,11,13,20,25,29] PP3300_PCH → PP3300_PCH

Quanta Computer Inc.
PROJECT : A23

| Size | Document Number | Rev. |
|---|---|---|
| C | PCH 4/6 (GPIO/MISC) | 1A |
| Date: Friday, August 16, 2013 | Sheet : 10 of 42 | |

## PCH VCCHSIO Power

PP1050_PCH reserve L39 *80/5A +V1.05DX_MODPHY

PP5000 U40 SLG59M1470VTR

C607 2 1 0.1U/10V/X5R_4 — C601 2 1 1U/6.3V/X5R_4 — PP1050_PCH_SUS

VDD GND D_01 S_01 D_02_03 S_02_03 ON

R560 *0/J_8S — R559 *0/J_8S — C602 0.1U/10V/X5R_4

PP3300_PCH PP3300_DSW

R604 100K/J_4 R228 *100K/J_4 R596 *0/J_4S R230 *100K/J_4 C608 0.047u/25V/X7R_4

[10] MODPHY_EN

check this foorpint

## Haswell ULT PCH (Power)

U42M HSW_ULT_DDR3L

HSIO: VCCHSIO K9, VCCHSIO L10, VCCHSIO M9, VCC1_05 N8, VCC1_05 P9, VCCUSB3PLL B18, VCCSATA3PLL B11

OPI: RSVD Y20, VCCAPLL AA21, VCCAPLL W21

USB3: DCPSUS3 J13

HDA: VCCHDA AH14

VRM: DCPSUS2 AH13

CORE: VCCSUS3_3 AC9, VCCSUS3_3 AA9, VCCSUS3_3 AH10, VCCDSW3_3 V8, VCC3_3 W9

GPIO/LPC: VCCCLK J18, VCCCLK K19, VCCACLKPLL A20, VCCCLK J17, VCCCLK R21, VCCCLK T21, VCCCLK K18, RSVD M20, RSVD V20, RSVD AE20, VCCSUS3_3 AE21, VCCSUS3_3

LPT LP POWER

RTC: VCCSUS3_3 AH11, VCCRTC AG10, DCPRTC AE7

SPI: VCCSPI Y8

USB3: VCCASW AG14, VCCASW AG13

HDA: VCC1_05 J11, VCC1_05 H11, VCC1_05 H15, VCC1_05 AE8, VCC1_05 AF22, VCC1_05 AG19, DCPSUSBYP AG20, DCPSUSBYP AE9, VCCASW AF9, VCCASW AG8, VCCASW AD10, DCPSUS1 AD9, DCPSUS1

CORE: VCCTS1_5 J15, VCC3_3 K14, VCC3_3 K16

THERMAL SENSOR

SERIAL IO: VCCSDIO U8, VCCSDIO T9

SUS OSCILLATOR

USB2: DCPSUS4 AB8, RSVD AC20, VCC1_05 AG16, VCC1_05 AG17

13 OF 19

### Power rails and components

+V1.05DX_MODPHY: C577 *1U/6.3V/X5R_4, C163 1U/6.3V/X5R_4, C175 1U/6.3V/X5R_4

PP1050_PCH: R179 *0/J_8S, C181 *1U/6.3V/X5R_4 — 1.741A

+V1.05S_AUSB3PLL: L18 2.2uH/210mA_8, C88 22u/6.3V/X5R_8, C77 22u/6.3V/X5R_8, C595 1U/6.3V/X5R_4 — 41mA

+V1.05S_ASATA3PLL: L17 2.2uH/210mA_8, C89 22u/6.3V/X5R_8, C79 22u/6.3V/X5R_8, C596 1U/6.3V/X5R_4 — 42mA

4/23 modify,Intel suggest 0 ohm

+V1.05S_APLLOPI: R6548 *0/J_8S, C248 *47u/6.3V/X5R_8, C619 *47u/6.3V/X5R_8, C218 1U/6.3V/X5R_4 — 57mA

+V1.05S_AIDLE — 1.838A

+1.05V_DCPSUS3: C177 *10u/6.3V/X5R_6, C166 *1U/6.3V/X5R_4 — 11mA

+1.05V_DCPSUS2: C235 *1U/6.3V/X5R_4

+V3.3DX_1.5DX_1.8DX_AUDIO: PP3300_PCH R252 0/J_6, PP1500_PCH_TS R260 *0/J_6, C234 0.1U/10V/X5R_4 Place close to ball

+VCCDSW +V3.3S_VCCPCORE

PP3300_PCH_SUS: C270 22u/6.3V/X5R_8 — 0.114A

Deep Sx / Non Deep Sx

PP3300_DSW: R254 *0/J_6S

PP3300_PCH_SUS: R253 *0/J_6, C238 1U/6.3V/X5R_4

PP3300_PCH: R165 *0/J_8S, C174 22u/6.3V/X5R_8 — 41mA

+V1.05S_AXCK_DCB: PP1050_PCH R6546 *0/J_8S, C579 47u/6.3V/X5R_8, C578 *47u/6.3V/X5R_8, C158 1U/6.3V/X5R_4 — 0.2A

+V1.05S_AXCK_LCPLL: PP1050_PCH R6547 *0/J_8S, C68 47u/6.3V/X5R_8, C76 *47u/6.3V/X5R_8, C594 1U/6.3V/X5R_4 — 31mA

0412 MOW-WW15 a 0.47uF cap between VccDSW3_3 and DcpSusByp is required if the 1.9A inrush current requirement cannot meet

PP1050_PCH: R6543 *0/J_6/1.05S_SSCF100, C164 1U/6.3V/X5R_4

PP1050_PCH: R6544 *0/J_6S +V1.05S_SSCFF, C209 1U/6.3V/X5R_4

PP3300_PCH_SUS — 63mA

R197 *0/J_6S C220 1U/6.3V/X5R_4 PP3300_PCH_SUS

PP3300_RTC: C642 1U/6.3V/X5R_4, C643 0.1U/10V/X5R_4, C231 0.1U/10V/X5R_4

+V3.3A_DSW_PRTCSUS

+VCCRTCEXT C208 0.1U/10V/X5R_4 — 18mA

R220 *0/J_6 PP3300_DSW, R204 *0/J_6S PP3300_PCH, C216 0.1U/10V/X5R_4 — 7/12 modify for leakage

+V3.3M_PSPI

PCH_VCC_1_1_20 R212 *0/J_6S PP1050_PCH, PCH_VCC_1_1_21 R194 *0/J_6S PP1050_PCH — 4/22 modify

place near CPU 4/23 modify, change short PAD

+V1.05S_CORE_PCH: R174 *short_8 PP1050_PCH, C192 10u/6.3V/X5R_6, C213 1U/6.3V/X5R_4, C237 1U/6.3V/X5R_4

+PCH_VCCDSW: C4 0.47u/25V/X7R_8 VCCPDSW, C233 1U/6.3V/X5R_4

+V1.05M_VCCASW: R217 *0/J_8S PP1050_PCH, C217 22u/6.3V/X5R_8, C221 1U/6.3V/X5R_4 — 0.658A

+1.05V_DCPSUS1 — 0.109A

+V1.5S_VCCATS: C212 *1U/6.3V/X5R_4 — 3mA

+V3.3S_VCCPTS: R111 *0/J_6S PP1500_PCH_TS, R107 *0/J_6S PP3300_PCH, C183 1U/6.3V/X5R_4 — 1mA

+V3.3S_VCCSDIO: R158 *0/J_6S PP3300_PCH, C194 1U/6.3V/X5R_4 — 17mA

+1.05V_DCPSUS4: C197 *1U/6.3V/X5R_4

+V1.05S_VCCUSBCORE: R270 *0/J_8S PP1050_PCH, C236 1U/6.3V/X5R_4

| | | |
|---|---|---|
| [8,13,31] | PP1050_PCH_SUS | PP1050_PCH_SUS |
| [8,22,23,25,26,27,28] | PP3300_RTC | PP3300_RTC |
| [5,13,26,31] | PP1050_PCH | PP1050_PCH |
| [9] | +V1.05S_AUSB3PLL | +V1.05S_AUSB3PLL |
| [8] | +V1.05S_ASATA3PLL | +V1.05S_ASATA3PLL |
| [7,8,9,10,13,20,25,29] | PP3300_PCH_SUS | PP3300_PCH_SUS |
| [5,7,8,10,13,20,21,24,25,26,28,29,33] | PP3300_DSW | PP3300_DSW |
| [2,7,8,9,10,13,20,25,29] | PP3300_PCH | PP3300_PCH |
| [9] | +V1.05S_AXCK_LCPLL | +V1.05S_AXCK_LCPLL |
| [18,20,22,23,24,25,28,30,31,32,34] | PP5000 | PP5000 |

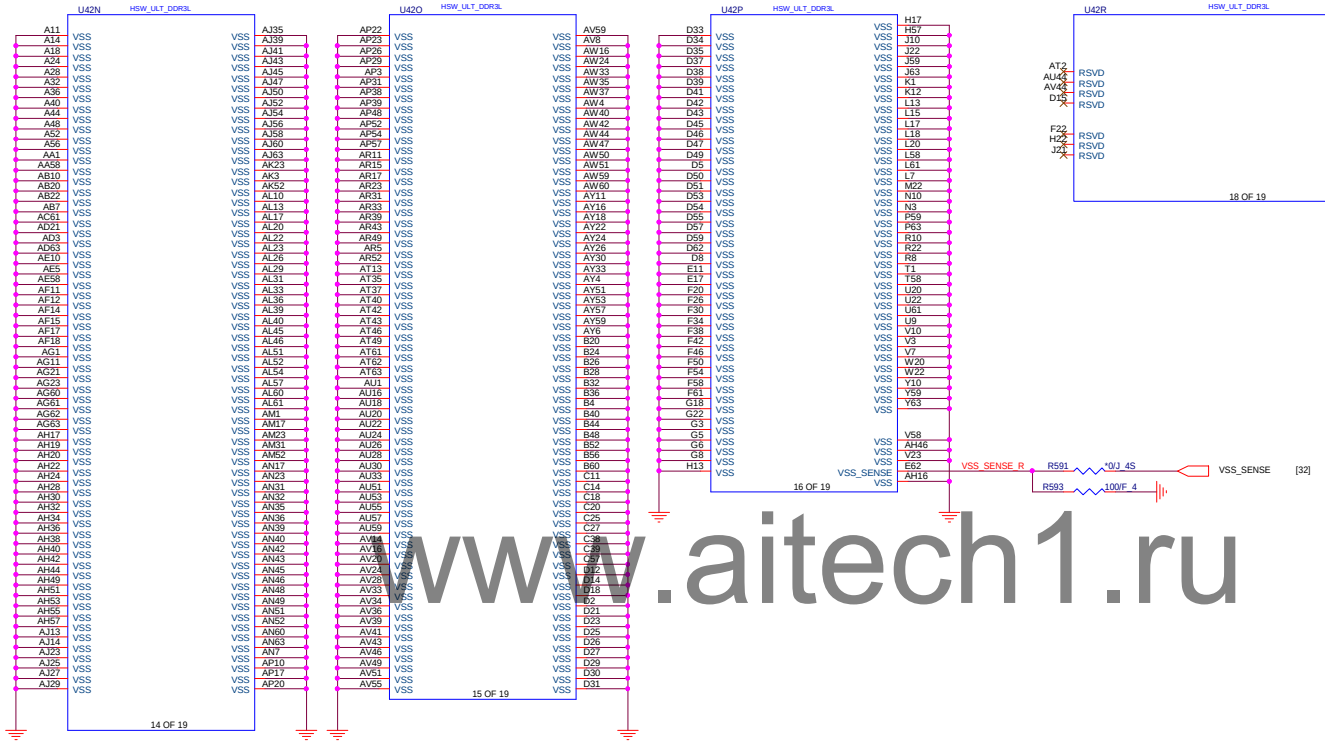


Quanta Computer Inc.

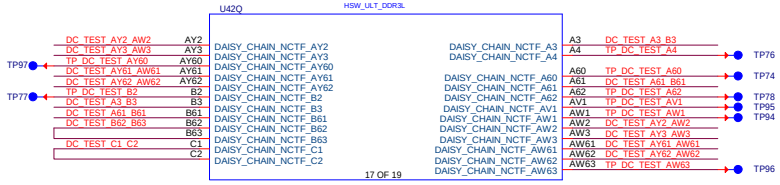
PROJECT : A23

| Size | Document Number | Rev. |
|---|---|---|
| C | PCH 5/6 (POWER) | 1A |
| Date: Friday, August 16, 2013 | Sheet : 11 of 42 | |

# Haswell ULT (GND)



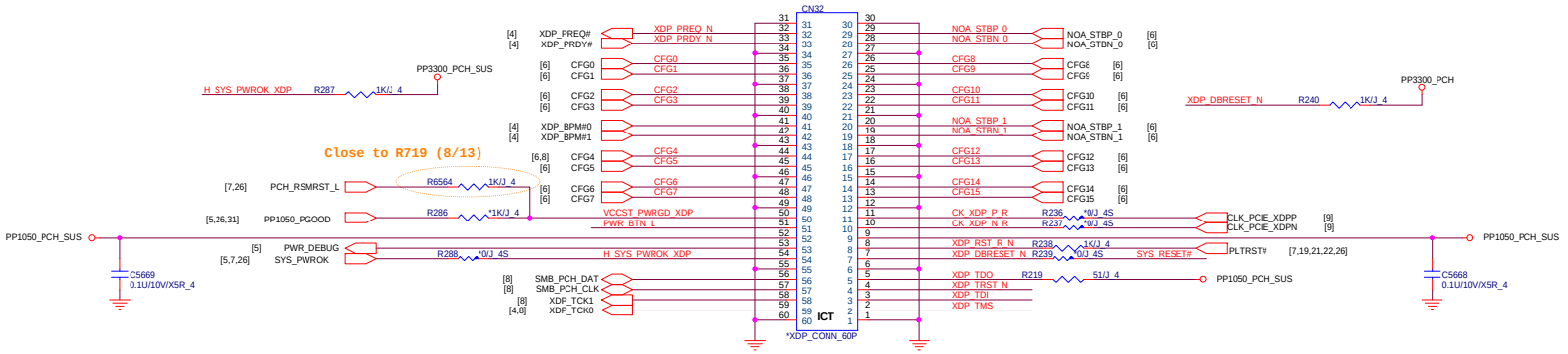


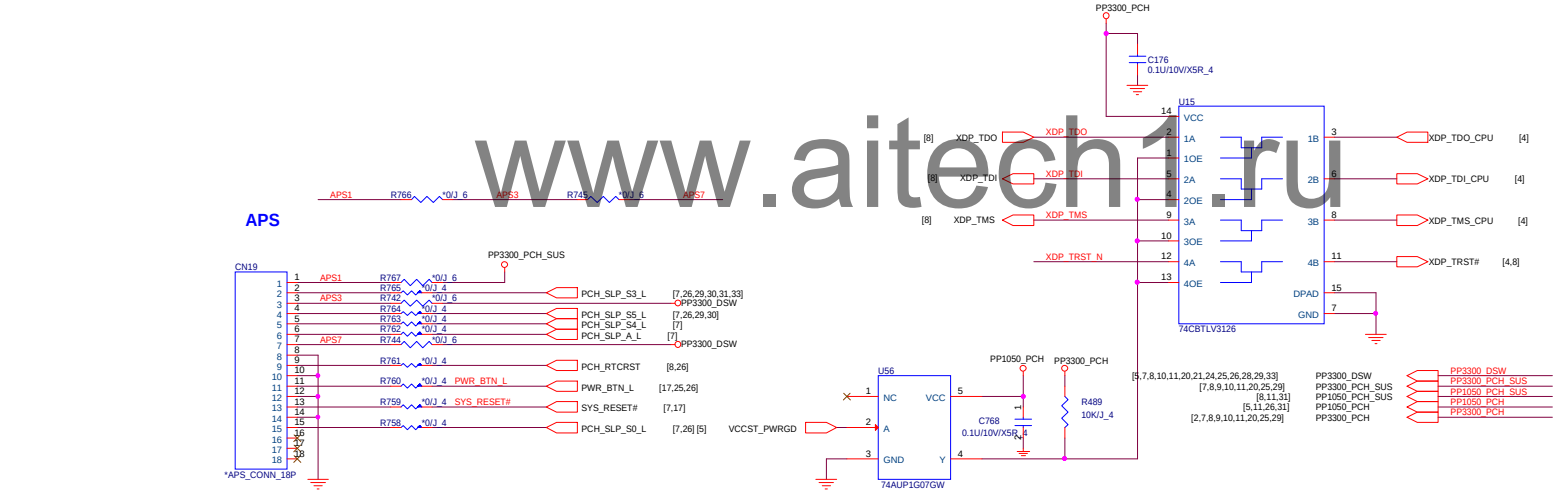




Quanta Computer Inc.

PROJECT : A23

| Size | Document Number | Rev. |
|---|---|---|
| C | PCH 6/6 (GND) | 1A |
| Date: Friday, August 16, 2013 | Sheet : 12 of 42 | |

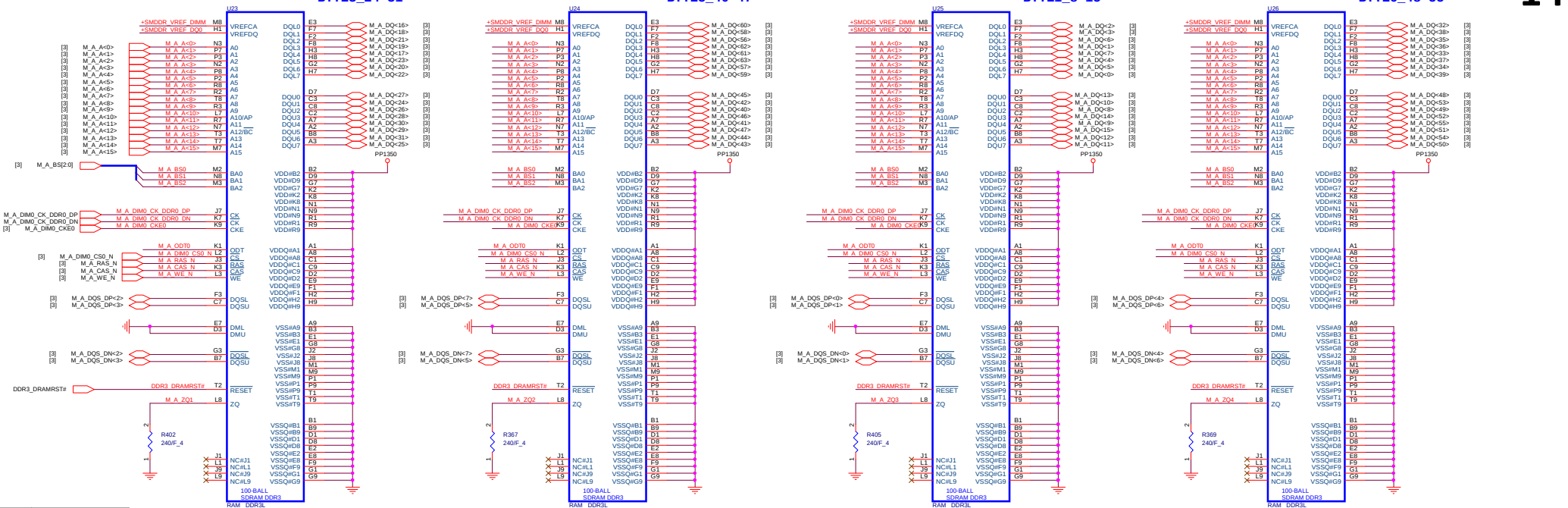





| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : A23 | | |
| Size: C | Document Number: CPU/PCH XDP | Rev: 1A |
| Date: Tuesday, August 20, 2013 | Sheet : 13 of 42 | |

BYTE2_16-23
BYTE3_24-31
BYTE7_56-63
BYTE5_40-47
BYTE0_0-7
BYTE1_8-15
BYTE4_32-39
BYTE6_48-55

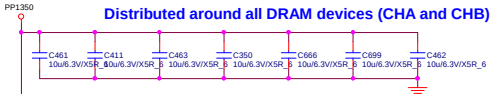



Micron/MT41K256M16HA-125:E/AKD5JGSTL02 for proto board

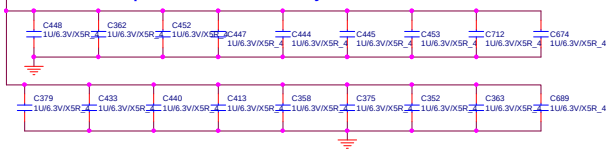
| Vendor | P/N | |
|---|---|---|
| Hynix | | |
| Elpida | AKD5JGST400 | DDR3L 1333Mhz 4Gb |
| | AKD5JGST404 | DDR3L 1600Mhz 4Gb |

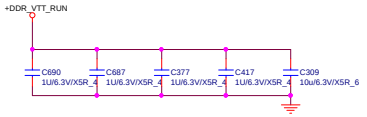


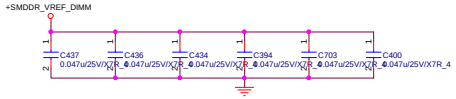
Distributed around all DRAM devices (CHA and CHB)



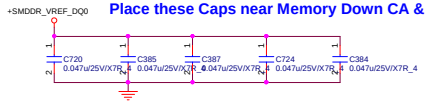

Place these Caps near each X16 Memory Down

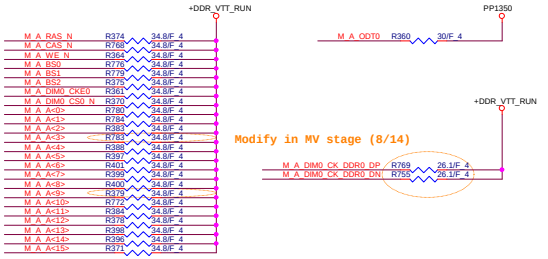


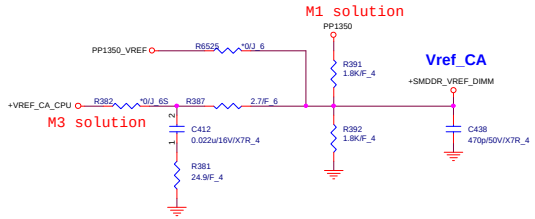




Place these Caps near Memory Down CA & DQ pin

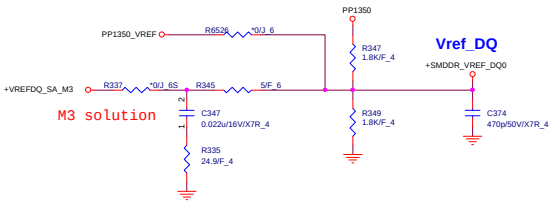



M1 solution




M1 solution

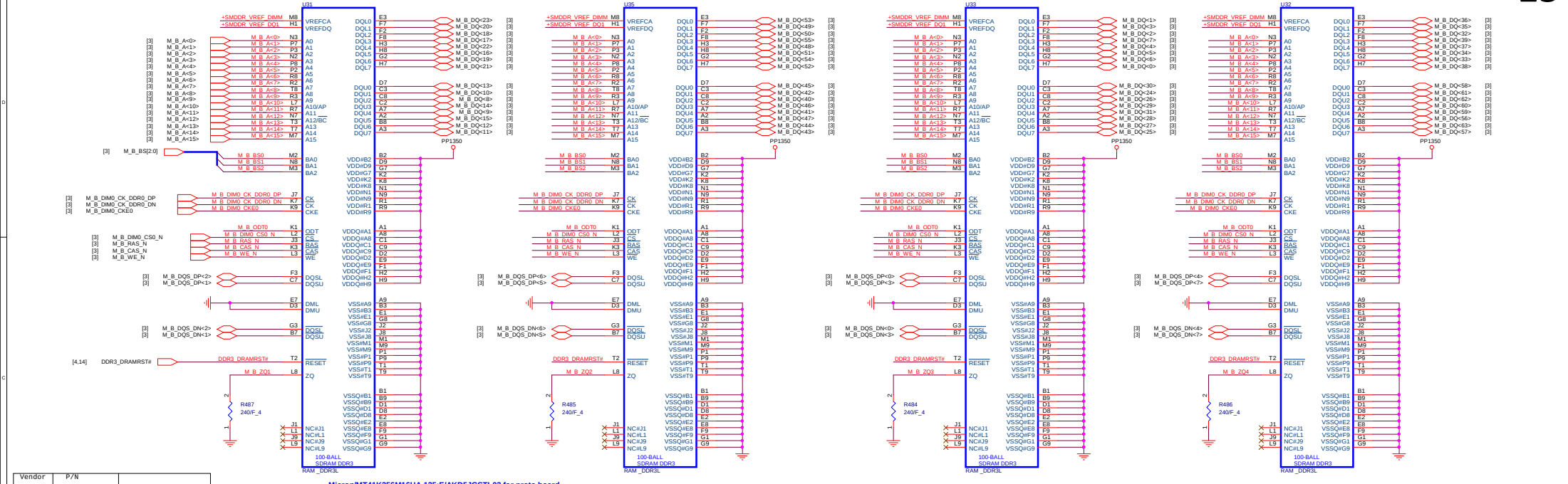



[3] +VREF_CA_CPU — +VREF_CA_CPU
[3] +VREFDQ_SA_M3 — +VREFDQ_SA_M3
[4,5,15,30] PP1350 — PP1350
[15,30] +DDR_VTT_RUN — +DDR_VTT_RUN
[15] +SMDDR_VREF_DIMM — +SMDDR_VREF_DIMM
[15,30] PP1350_VREF — PP1350_VREF

Quanta Computer Inc.
PROJECT : A23

| Size | Document Number | Rev. |
|---|---|---|
| Custom | DDR3L MEMORY DOWNx16 A | 1A |
| Date: Friday, August 16, 2013 | Sheet: 14 of 42 | |

BYTE1_8-15
BYTE2_16-23
BYTE5_40-47
BYTE6_48-55
BYTE0_0-7
BYTE3_24-31
BYTE4_32-39
BYTE7_56-63




Micron/MT41K256M16HA-125:E/AKD5JGSTL02 for proto board

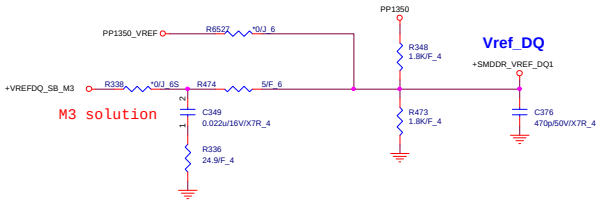
| Vendor | P/N | |
|---|---|---|
| Hynix | | |
| Elpida | AKD5JGST400 | DDR3L 1333Mhz 4Gb |
| | AKD5JGST404 | DDR3L 1600Mhz 4Gb |

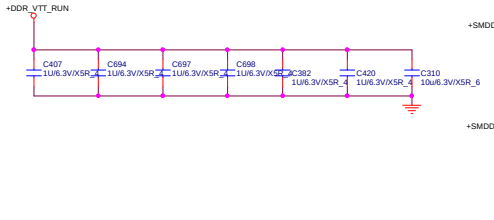


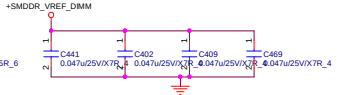

Place these Caps near each X16 Memory Down



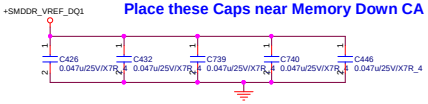

M1 solution

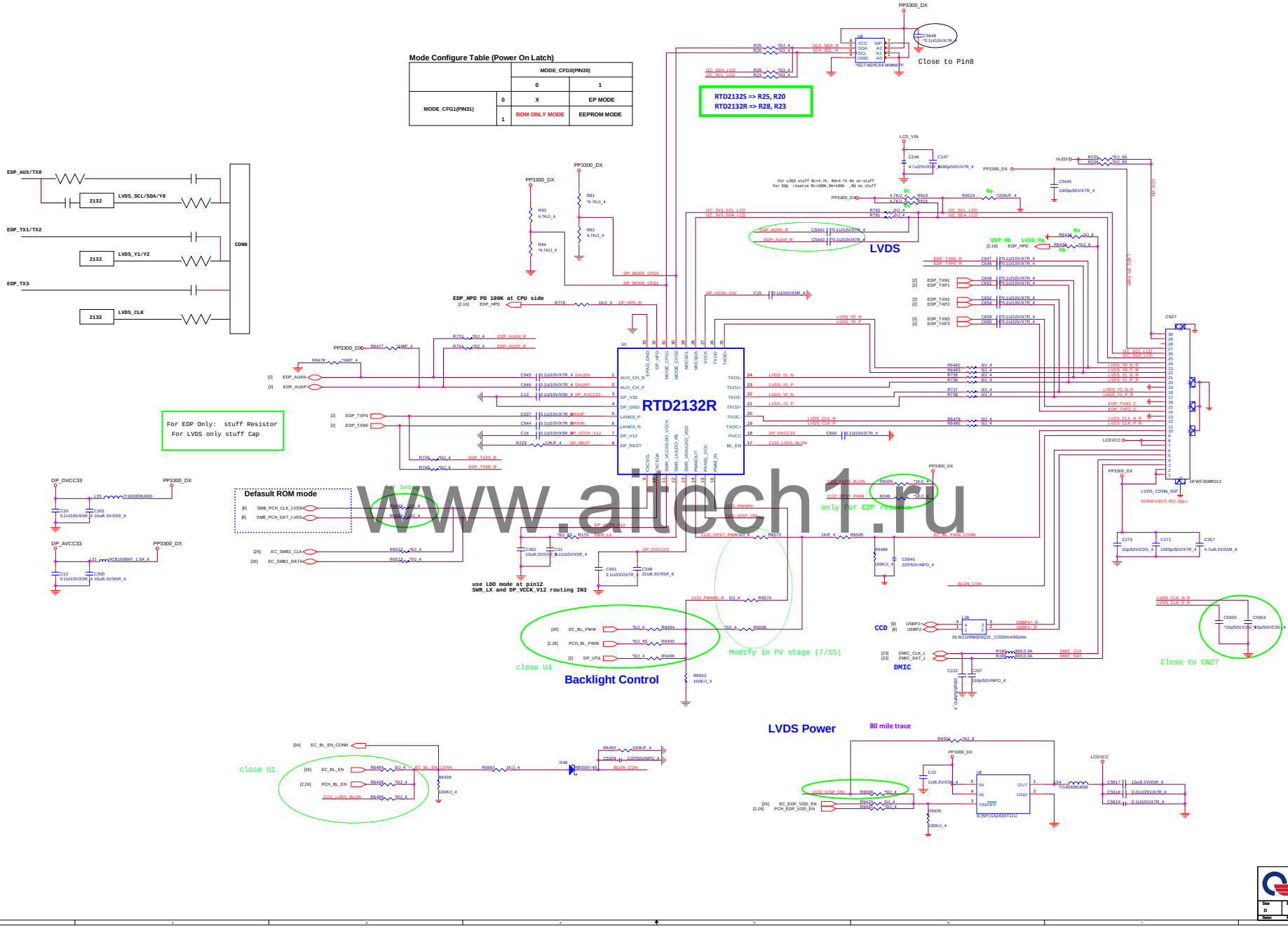



Place these Caps near Memory Down CA & DQ pin

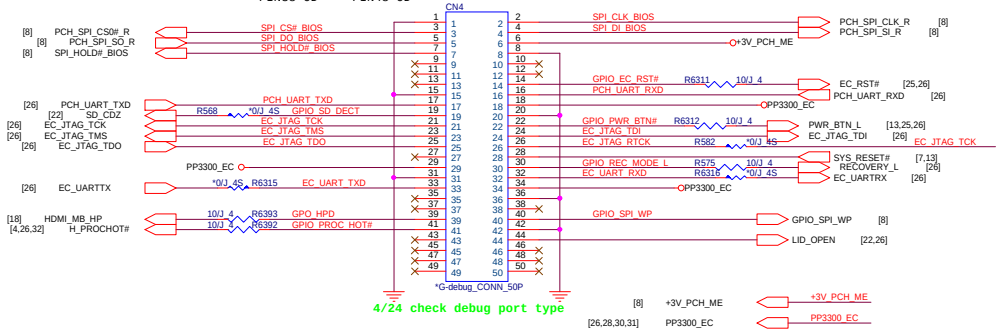



| | |
|---|---|
| Quanta Computer Inc. | |
| PROJECT : A23 | |
| Size: D | Document Number: LVDS/CAMERA/DMIC/RTD2132 |
| Rev: 1A | |
| Date: Friday, August 16, 2013 | Sheet: 16 of 42 |

# Debug Port

PIN7 OD
PIN14 OD
PIN19 OD
PIN22 OD
PIN28 OD
PIN30 OD
PIN37 OD
PIN38 OD
PIN39 OD
PIN41 OD
PIN43 OD
PIN44 OD
PIN45 OD
PIN46 OD
PIN47 OD
PIN48 OD
PIN49 OD
PIN50 OD



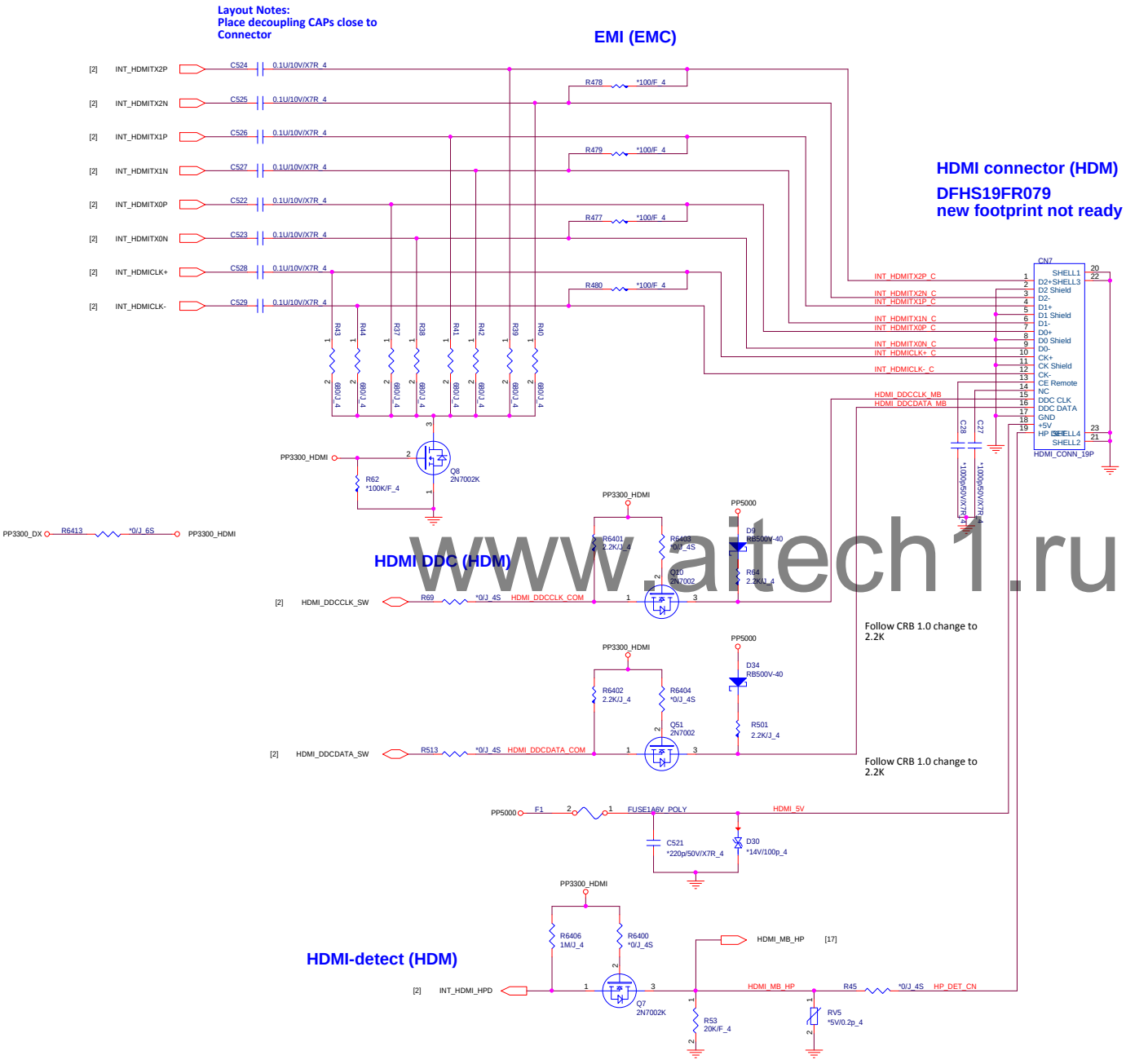

4/24 check debug port type



Quanta Computer Inc.

PROJECT : A23

| Size | Document Number | Rev. |
|---|---|---|
| C | Debug | 1A |
| Date: Friday, August 16, 2013 | Sheet : 17 of 42 | |






Quanta Computer Inc.

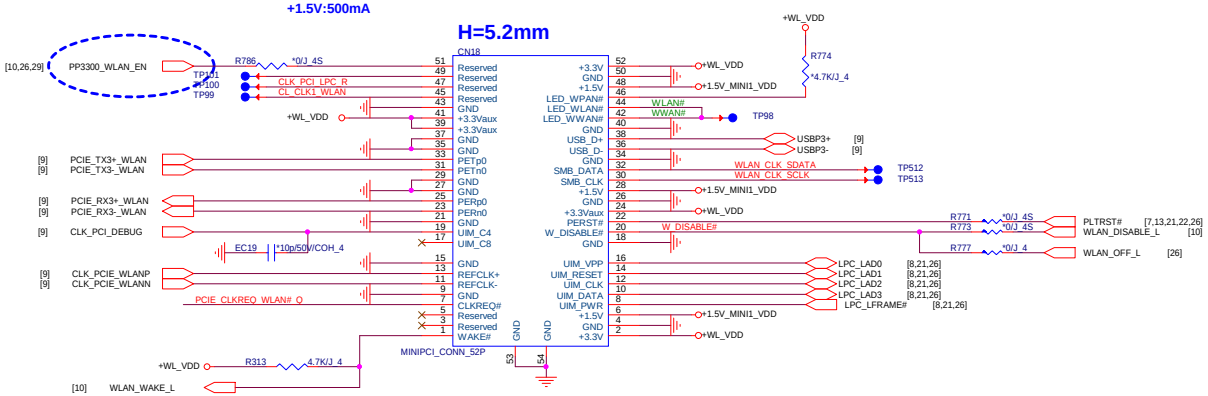
PROJECT : A23

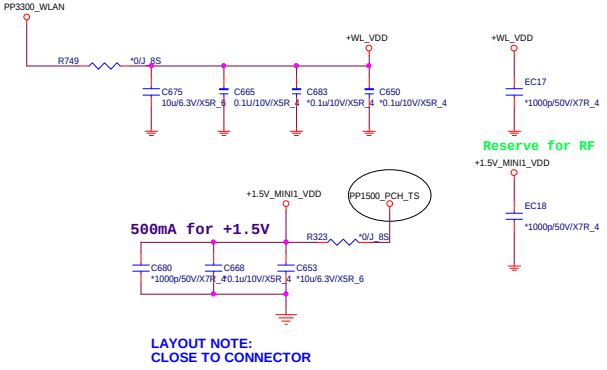
| Size | Document Number | Rev. |
|---|---|---|
| C | HDMI | 1A |
| Date: Friday, August 16, 2013 | Sheet : 18 of 42 | |

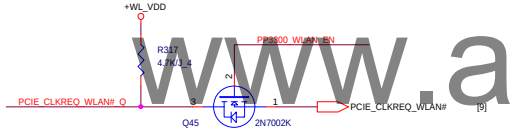
## MINI-CARD WLAN(MPC)

+3.3V: 1000mA
+3.3Vaux:330mA
+1.5V:500mA

H=5.2mm



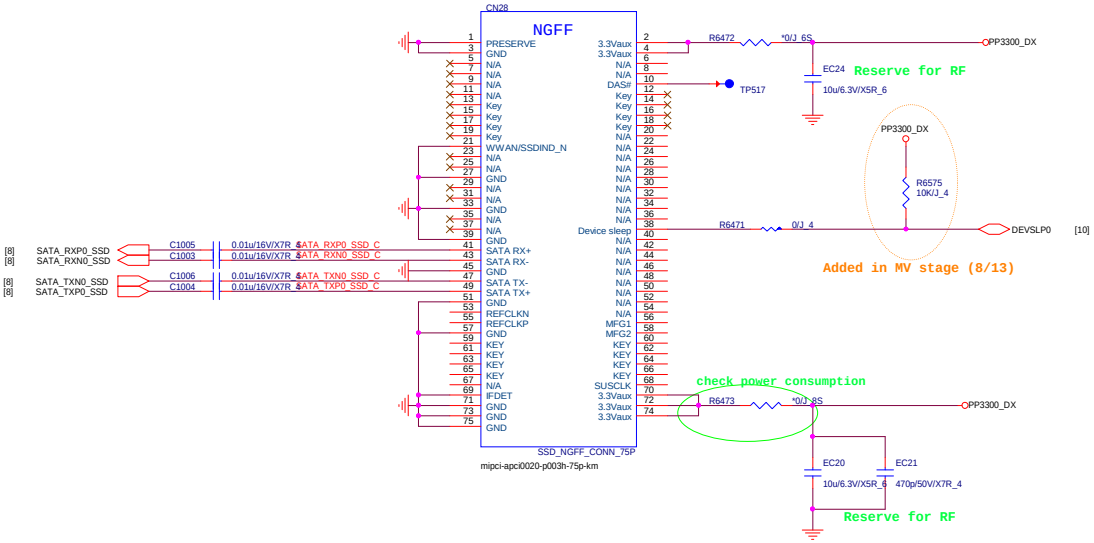

PP1500_PCH_TS
PP3300_WLAN



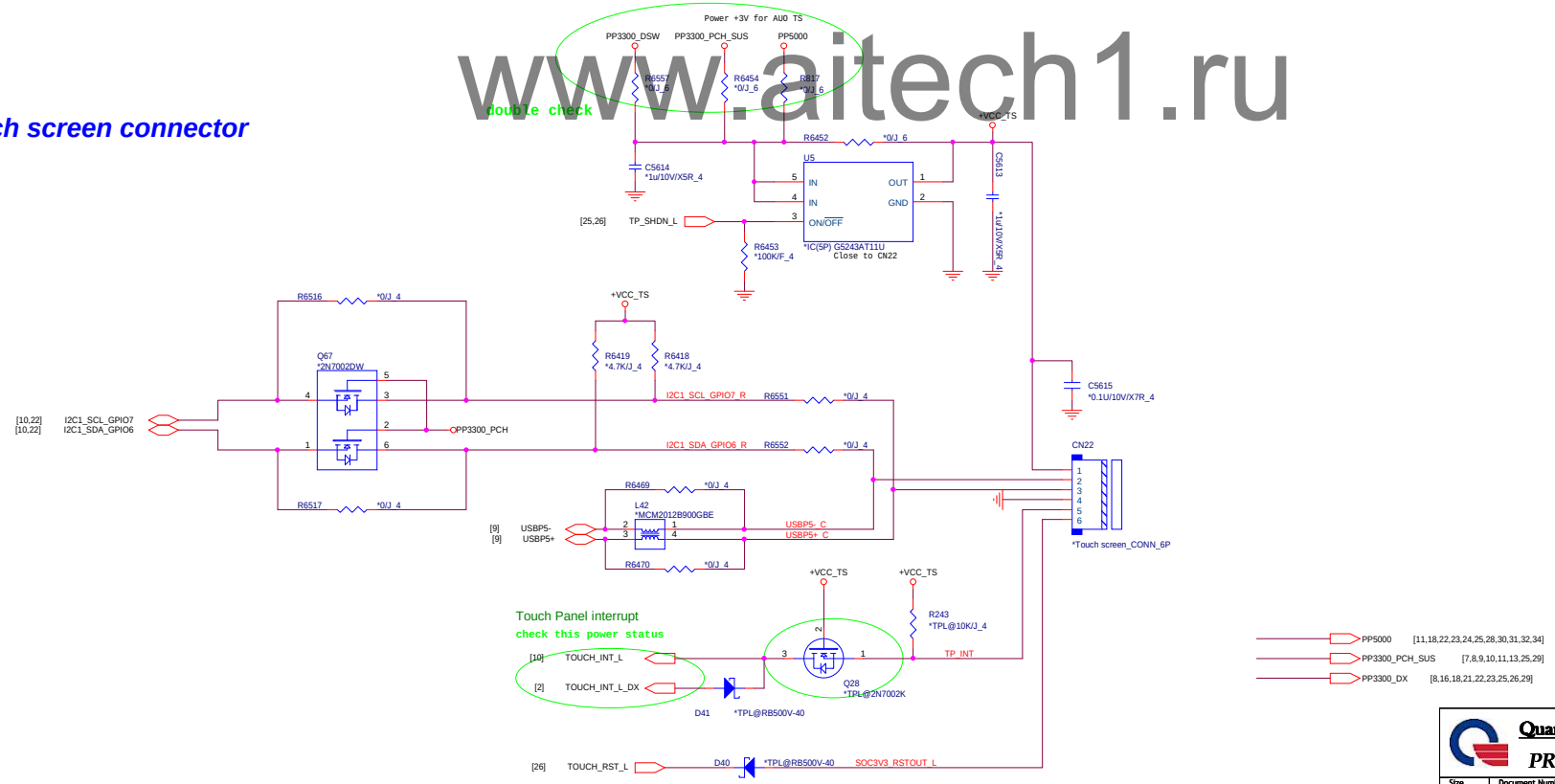
Quanta Computer Inc.
PROJECT : A23

| Size | Document Number | Rev. |
|---|---|---|
| C | WIFI / BT | 1A |
| Date: Friday, August 16, 2013 | Sheet : 19 of 42 | |

| pin | Type | Description |
|---|---|---|
| 1 | PRESENCE | This pin is grounded on the SSD. May be used by host to determine if slot is empty or populated |
| 10 | DAS# | Device Activity Signal |
| 21 | WWAN/SSDIND_N | This pin connect to Ground |
| 38 | Device Sleep Signal | If system didn't support DEVSLP, set DEVSLP Sleep Signal pin power high and keep (from power on), device will ignore.<br>If system support DEVSLP, set DEVSLP Sleep Signal pin power low (from power on) device, device will support DEVSLP function.<br>Device Sleep Signal H: SSD enter sleep model.<br>Device Sleep Signal L: SSD exit sleep model. |
| 53 | REFCLKN | no connect on SSD |
| 55 | REFCLKP | no connect on SSD |
| 56 | MFG1 | Manufacturing pin. Use determined by vendor. Must be a noconnect on the host board |
| 58 | MFG2 | Manufacturing pin. Use determined by vendor. Must be a noconnect on the host board |
| 68 | SUSCLK | no connect on SSD |
| 69 | IFDET | This pin connect to Ground |




## Touch screen connector



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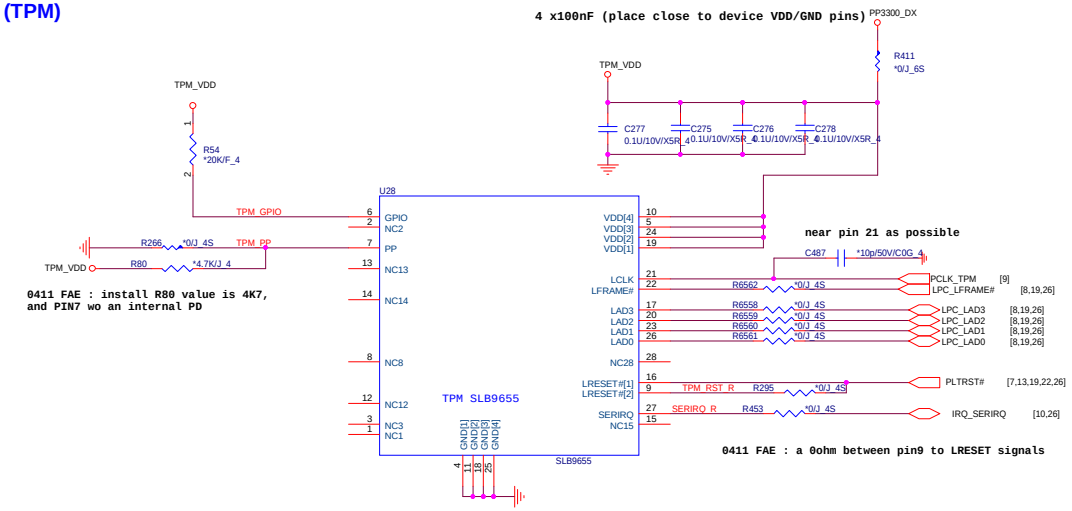
PROJECT : A23

| Size | Document Number | Rev. |
|---|---|---|
| C | SSD/TS /ALS | 1A |
| Date: Friday, August 16, 2013 | Sheet : 20 of 42 | |

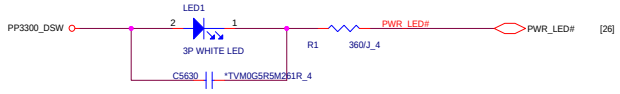
## TPM (TPM)




## LED(UIF)



### PWR LED




PP3300_DSW [5,7,8,10,11,13,20,24,25,26,28,29,33]
PP3300_DX [8,16,18,20,22,23,25,26,29]

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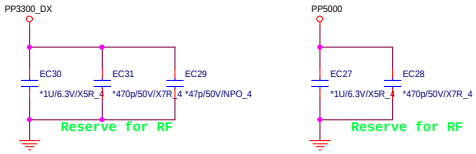
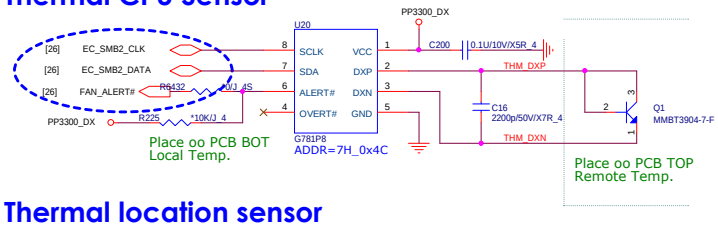
PROJECT : A23

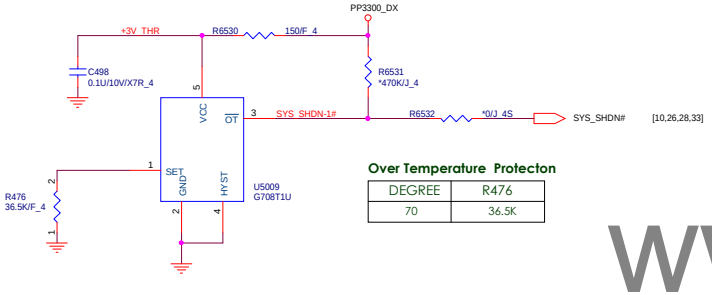
| Size | Document Number | Rev. |
|---|---|---|
| C | TPM SLB9655 / LED | 1A |
| Date: Friday, August 16, 2013 | Sheet : 21 of 42 | |




## Thermal CPU Sensor

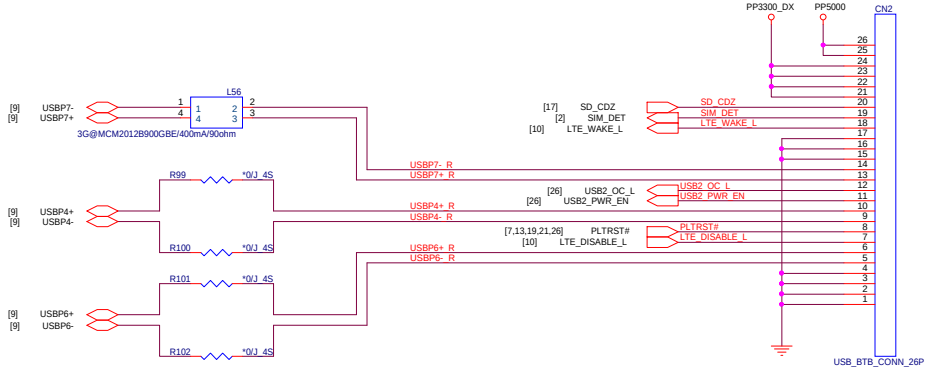



## Thermal location sensor



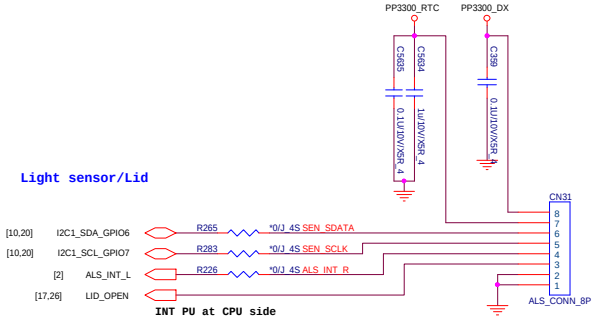

**Over Temperature Protecton**

| DEGREE | R476 |
|---|---|
| 70 | 36.5K |

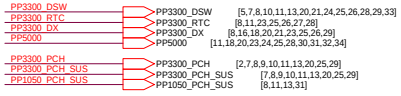



| | |
|---|---|
| USB 2.0<br>2A | +5V x2 |
| | USBP7+ |
| | USBP7- |
| | USB_OC3# |
| | USBON# |
| | GND x 2 |
| WWAN<br>3A | +3V x 3 |
| | USBP0+ |
| | USBP0- |
| | RF_KILL# |
| | PLTRST# |
| | GND x 4 |
| CR<br>1A | +3V x 1 |
| | USBP6+ |
| | USBP6- |
| | GND x 1 |






CN31 check footprint /pin define

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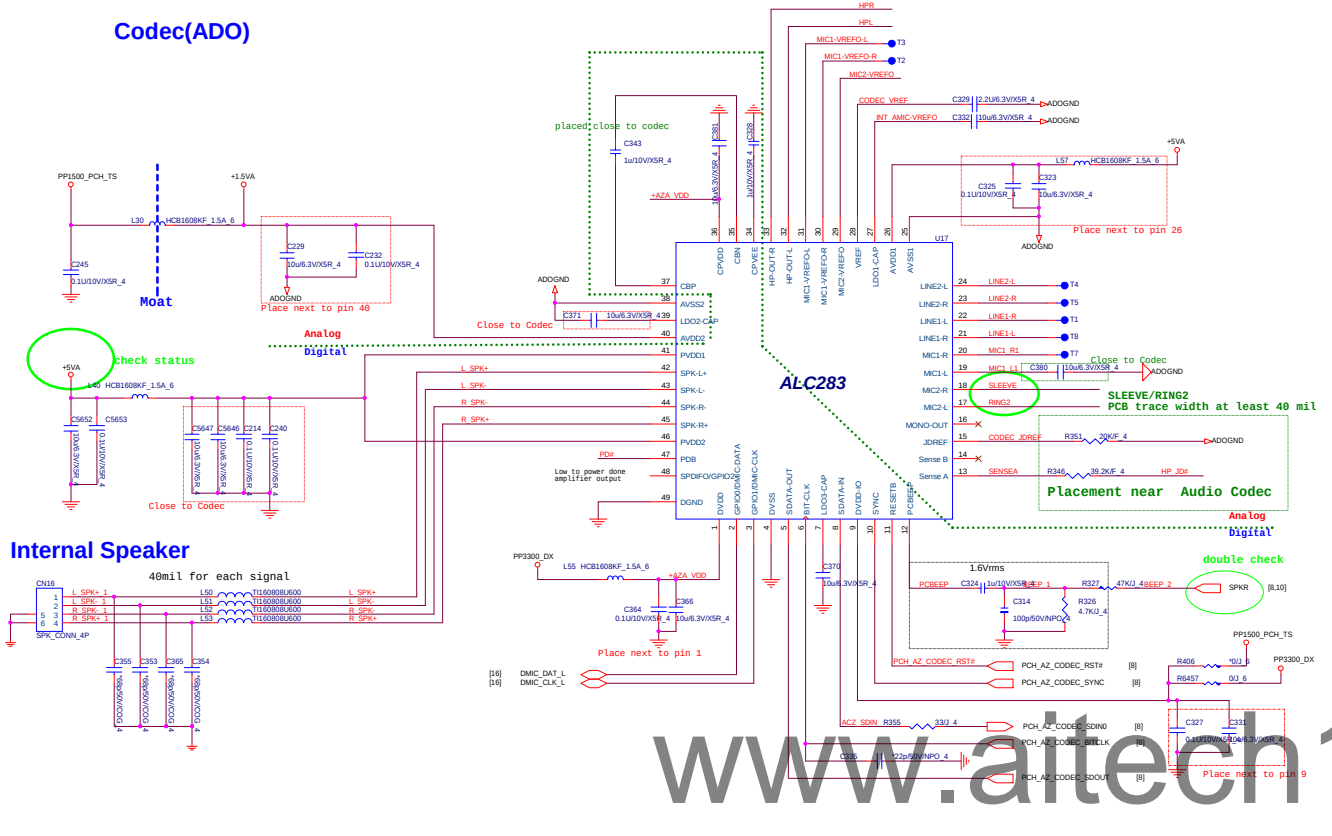
PROJECT : A23

| Size | Document Number | Rev. |
|---|---|---|
| C | USB2.0/WWAN/CR/ALS/Thermal IC | 1A |
| Date: Friday, August 16, 2013 | Sheet : 22 of 42 | |

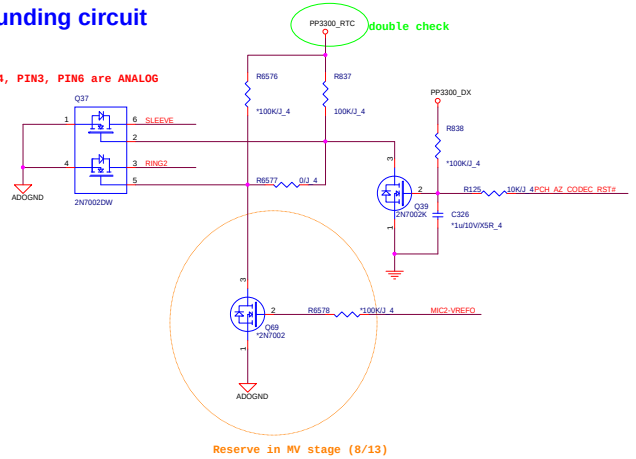
## Codec(ADO)




## Internal Speaker

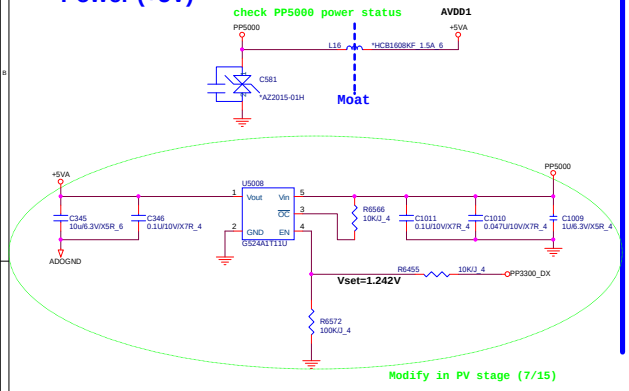



## Grounding circuit

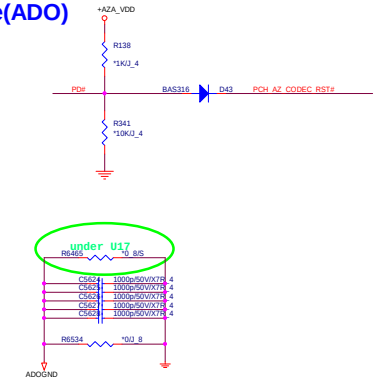




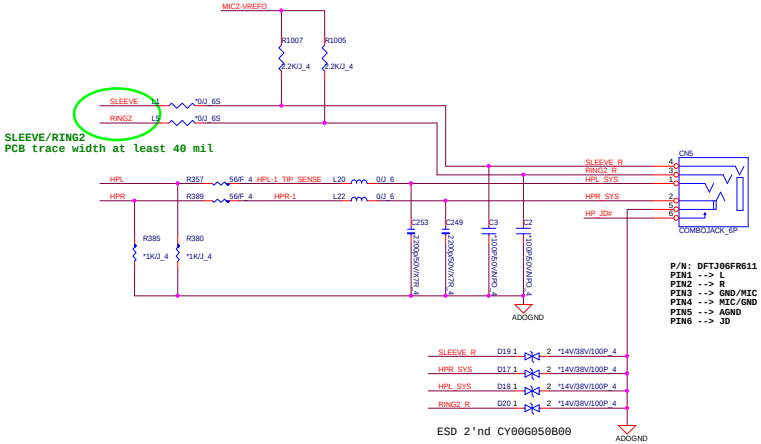

## Power (+5V)




## Mute(ADO)




## HEADPHONE/Mic Combo Jack

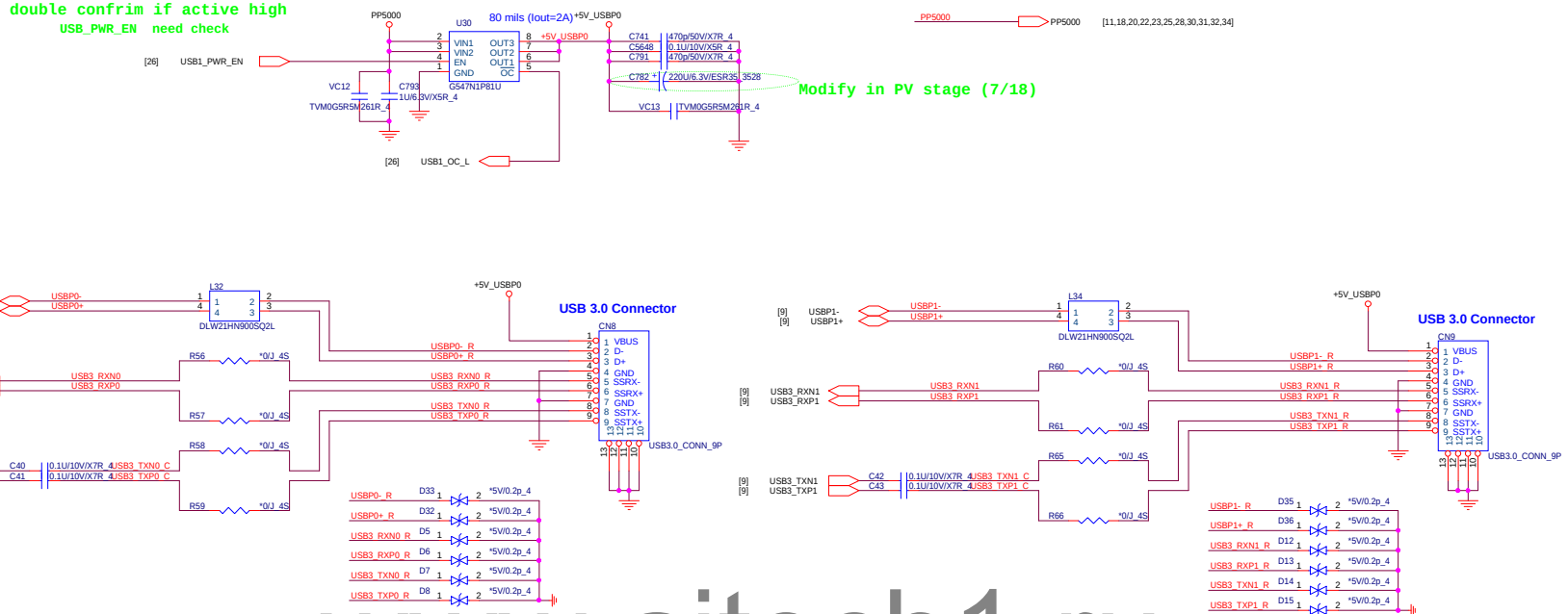



| | | |
|---|---|---|
| PP3300_DSW | PP3300_DSW | [5,7,8,10,11,13,20,21,24,25,26,28,29,33] |
| PP3300_RTC | PP3300_RTC | [8,11,22,25,26,27,28] |
| PP3300_DX | PP3300_DX | [8,16,18,20,21,22,25,26,29] |
| PP5000 | PP5000 | [11,18,20,22,24,25,28,30,31,32,34] |

Quanta Computer Inc.
PROJECT : A23

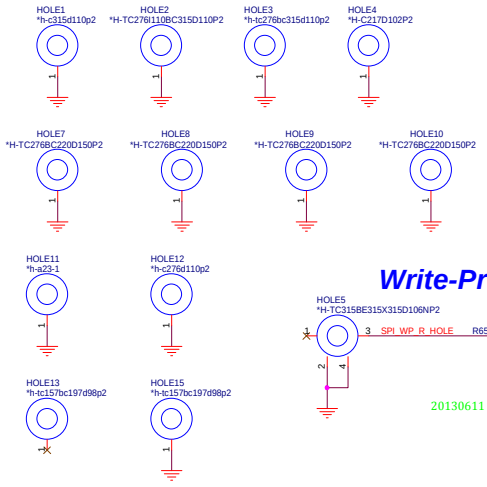
| Size | Document Number | Rev. |
|---|---|---|
| Custom | ALC283/HP/DMIC/SPK | 1A |
| Date: Monday, August 19, 2013 | Sheet : 23 of 42 | |

## USB3.0

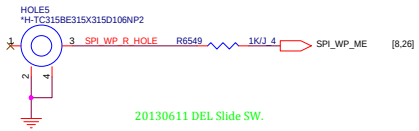


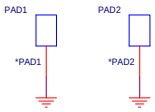



## HOLE(OTH)

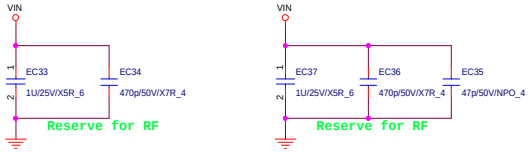



## Write-Protect Switch

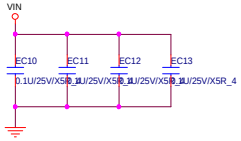


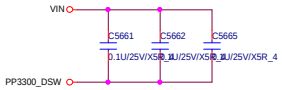

## RF Cap.

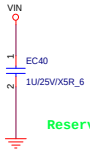



## EMI Cap.




## Cross Power Plan Cap.




| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : A23 | | |
| Size: C | Document Number: USB3/SW/Hole | Rev: 1A |
| Date: Friday, August 16, 2013 | Sheet : 24 of 42 | |

# TOUCHPAD BOARD CONN (TPD)

Add in PV stage (7/15)

Stuff in MV stage (8/13)

check this power status

Modify Net name in MV stage (8/13)

check pin define 0322

footprint 50506-00641-001-6p-l
DFFC06FR050

## K/B (KBC)

Check pin define 0321
DFFC30FR058
footprint 51510-03001-001-30p-l

Touch Panel interrupt

check power status

## KEYBOARD BACK LIGHT

Removed in PV stage (7/15)

## HOLELESS RESET 2-CHIP

modify no BATT_EN function

co-layout 4K4108 and 4K4137
SLG4K4108 (AL004108000)
SLG4K4137 (AL004137000)
4K4137 PIN3 is BATT_ENABLE
4K4137 PIN4 is AC_PRESENT

## CPU FAN1 (THM)

Connect to EC reset pin
Connect to GPIO on CPU with PU to GPIO power well
Connect to EC pin C5 (must be low when EC IN RESET)

check with PWM signal is 3V or 5V ,if 3V can skip some circuit

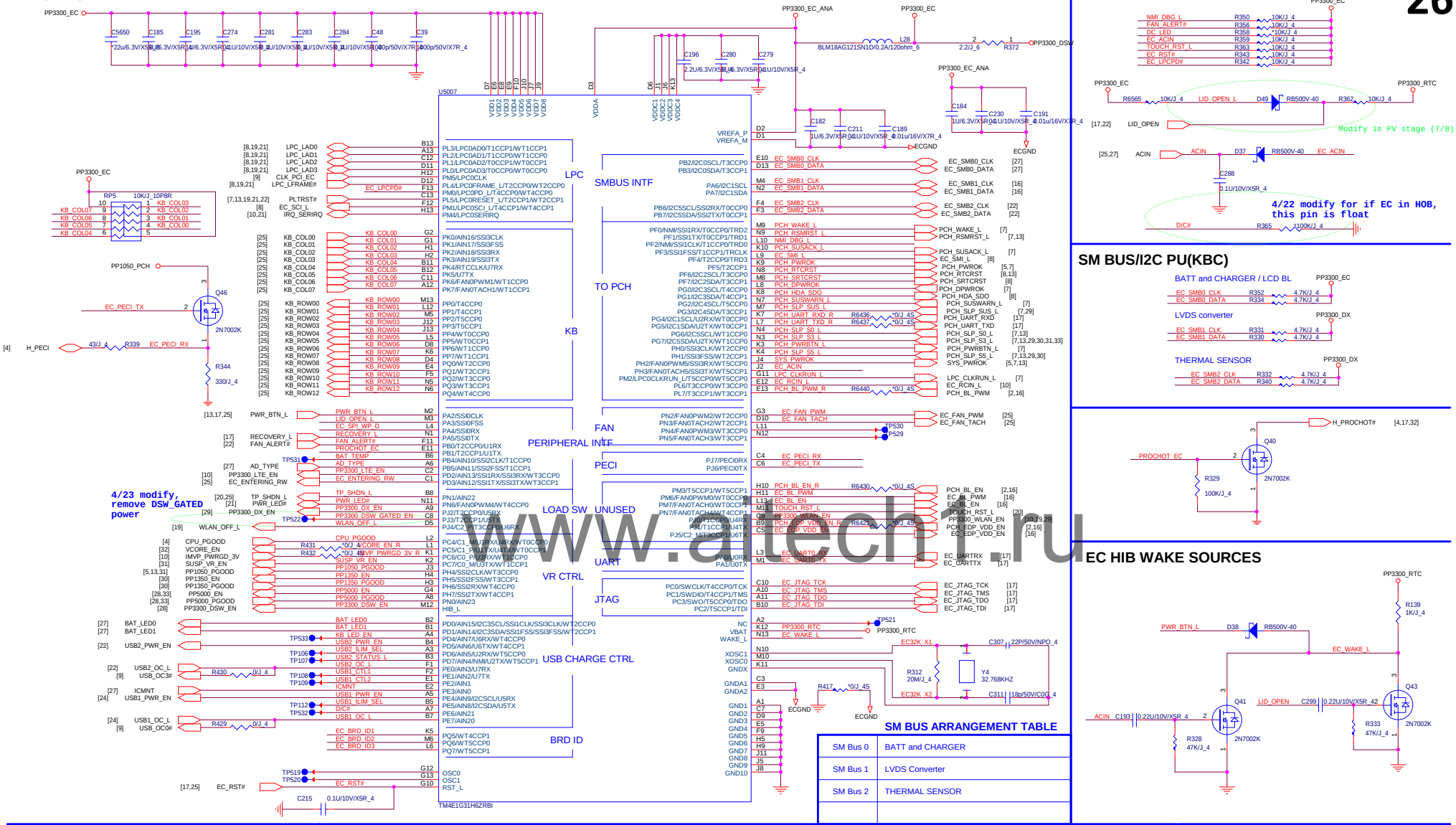
Check FAN power leakage



Quanta Computer Inc.
PROJECT : A23

| Size | Document Number | Rev. |
|---|---|---|
| C | KB/KB LIGHT/TP/FAN | 1A |
| Date: Friday, August 16, 2013 | Sheet : 25 of 42 | |

# EC(KBC)




## SM BUS/I2C PU(KBC)




## EC HIB WAKE SOURCES




### SM BUS ARRANGEMENT TABLE

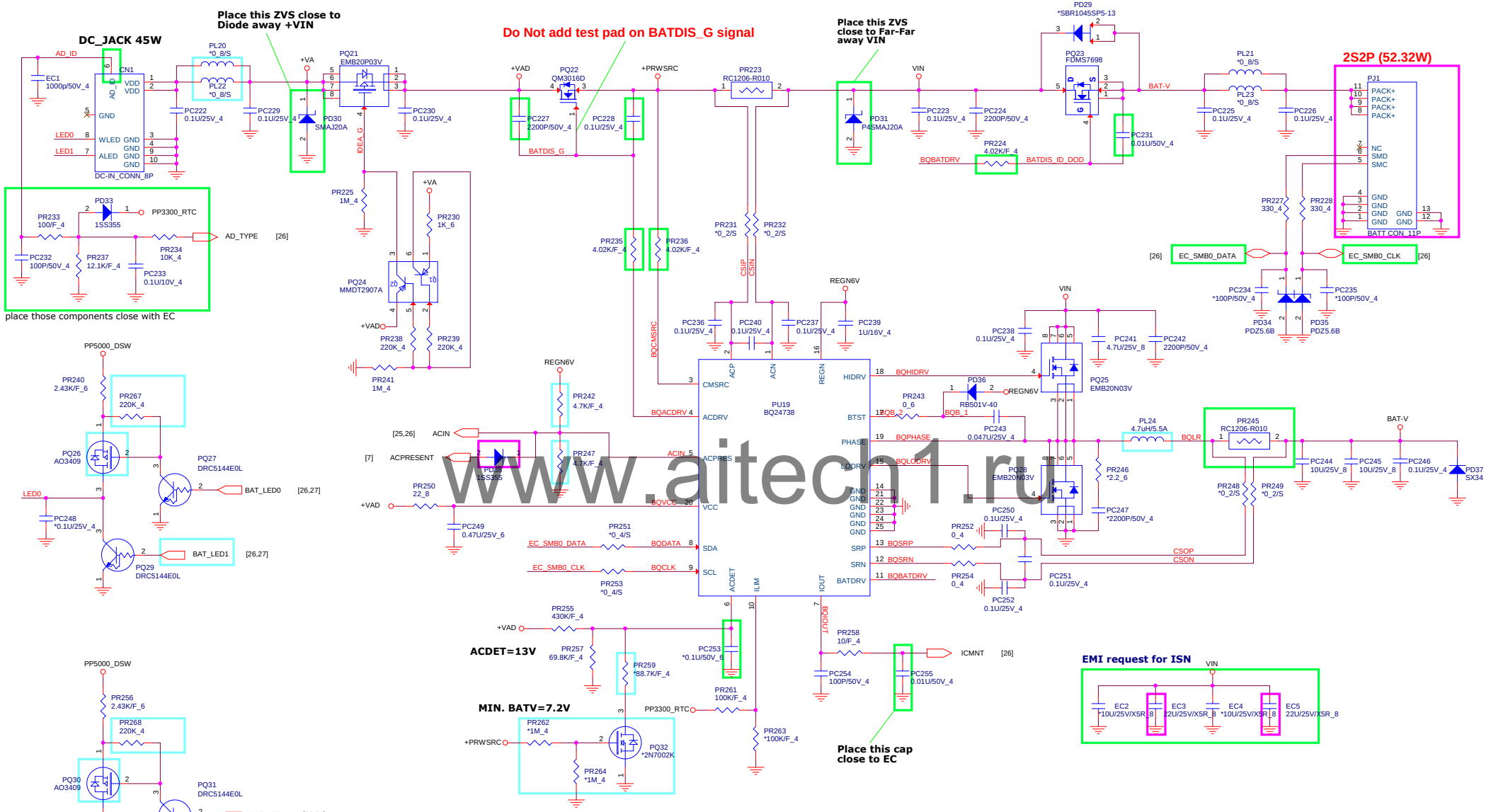
| | |
|---|---|
| SM Bus 0 | BATT and CHARGER |
| SM Bus 1 | LVDS Converter |
| SM Bus 2 | THERMAL SENSOR |
| | |

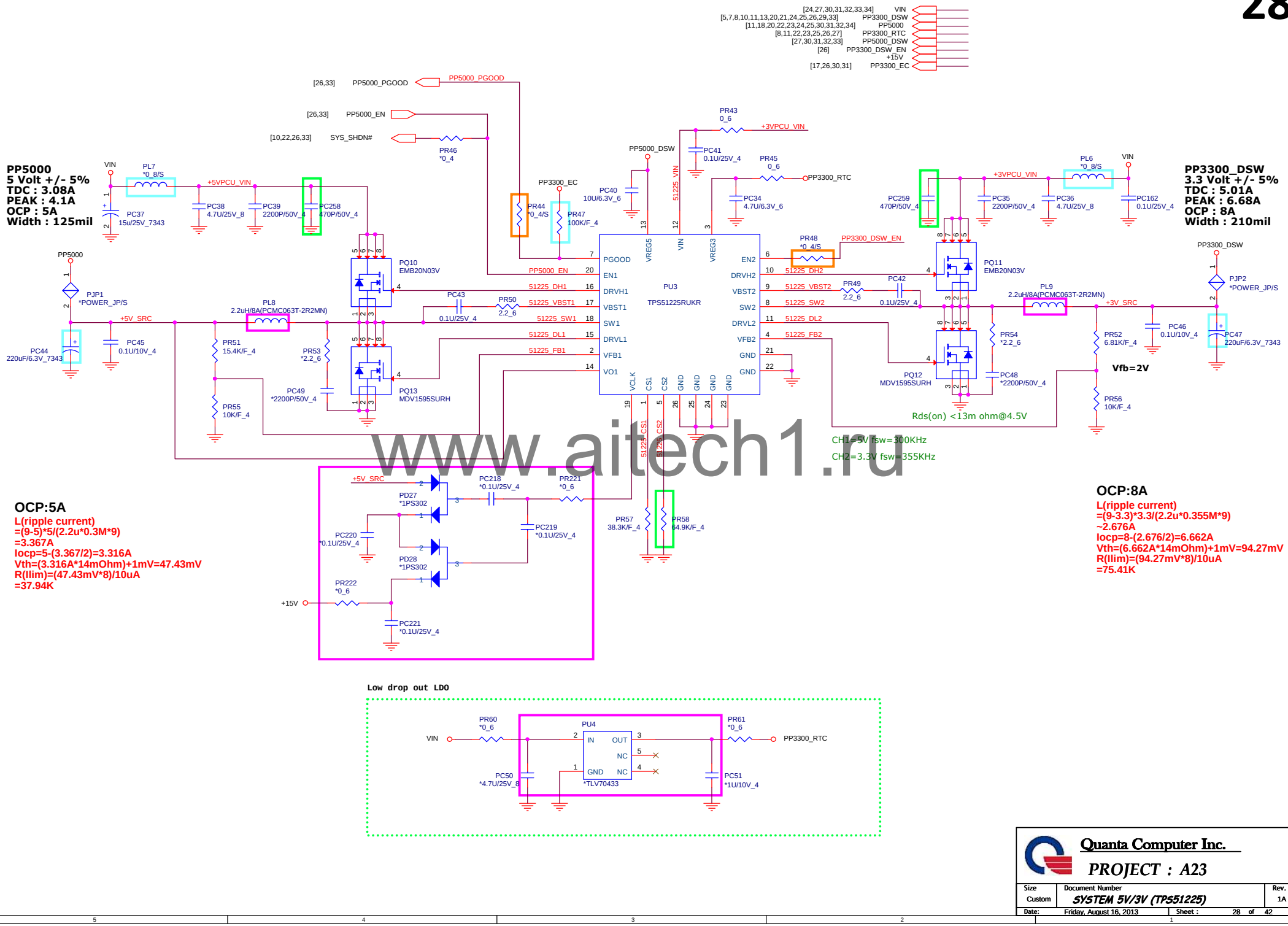


Quanta Computer Inc.

PROJECT : A23

| Size | Document Number | Rev. |
|---|---|---|
| C | KBC TI TM4E1G31H6ZRBI | 1A |
| Date: Friday, August 16, 2013 | Sheet : 26 of 42 | |



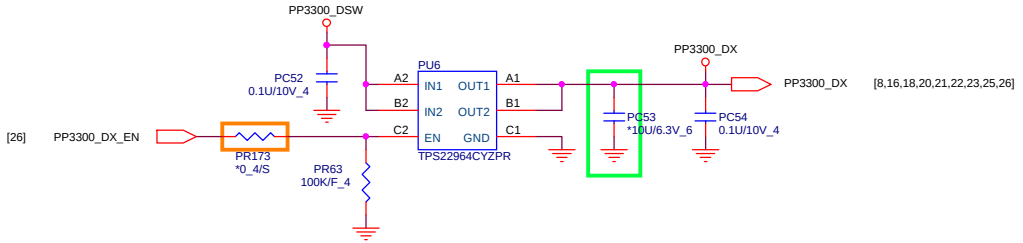


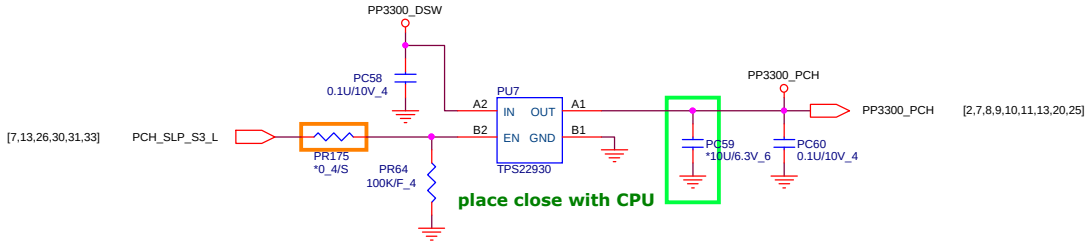



Quanta Computer Inc.

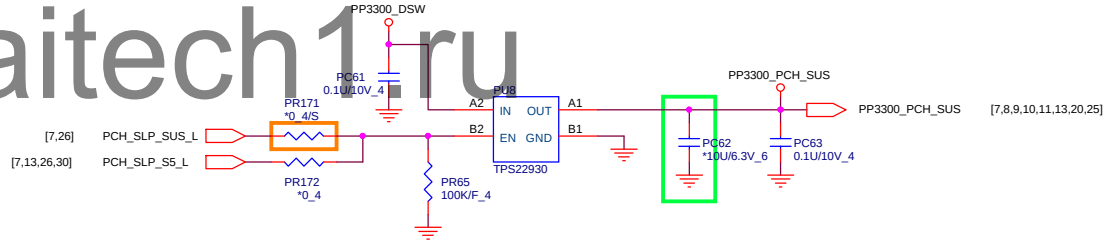
PROJECT : A23

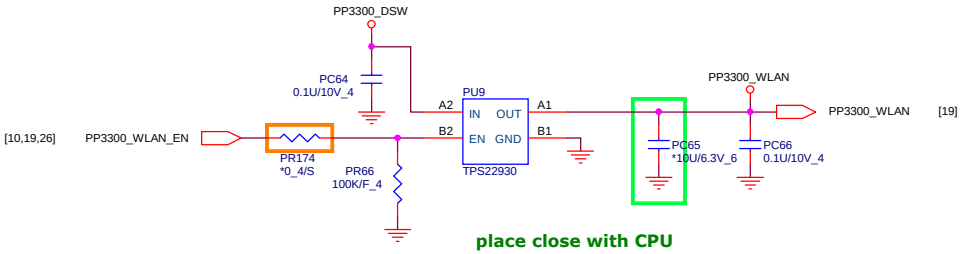
| Size | Document Number | Rev. |
|---|---|---|
| Custom | SYSTEM 5V/3V (TPS51225) | 1A |
| Date: Friday, August 16, 2013 | Sheet : 28 of 42 | |



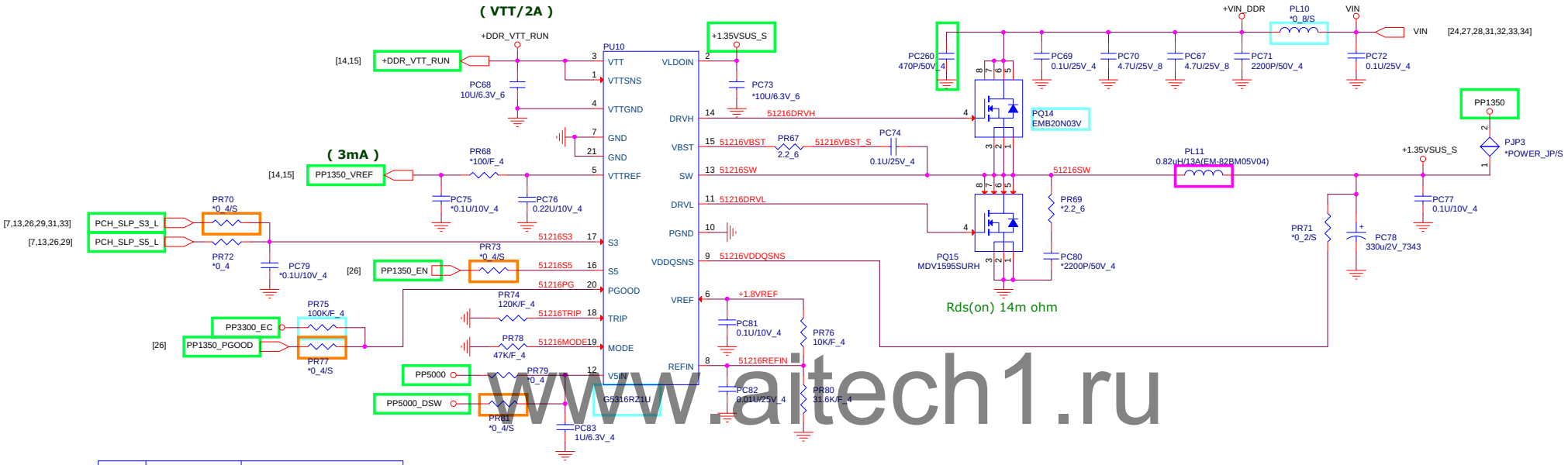



| | | |
|---|---|---|
| Quanta Computer Inc. | | |
| PROJECT : A23 | | |
| Size: Custom | Document Number: SYSTEM 5V/3V (TPS51225) | Rev: 1A |
| Date: Friday, August 16, 2013 | Sheet : 29 of 42 | |

**+1.35V +/- 5%**
**Countinue current:6A**
**Peak current:10A**
**OCP minimum:12A**






| Mode | Frequency | Discharge mode |
|---|---|---|
| 47K | 400K | non Tracking Discharge |

| | S3 | S5 | +1.35VSUS | REF | VTT |
|---|---|---|---|---|---|
| S0 | 1 | 1 | ON | ON | ON |
| S3 (mainon off) | 0 | 1 | ON | ON | OFF |
| S4/S5 | 0 | 0 | OFF | OFF | OFF |

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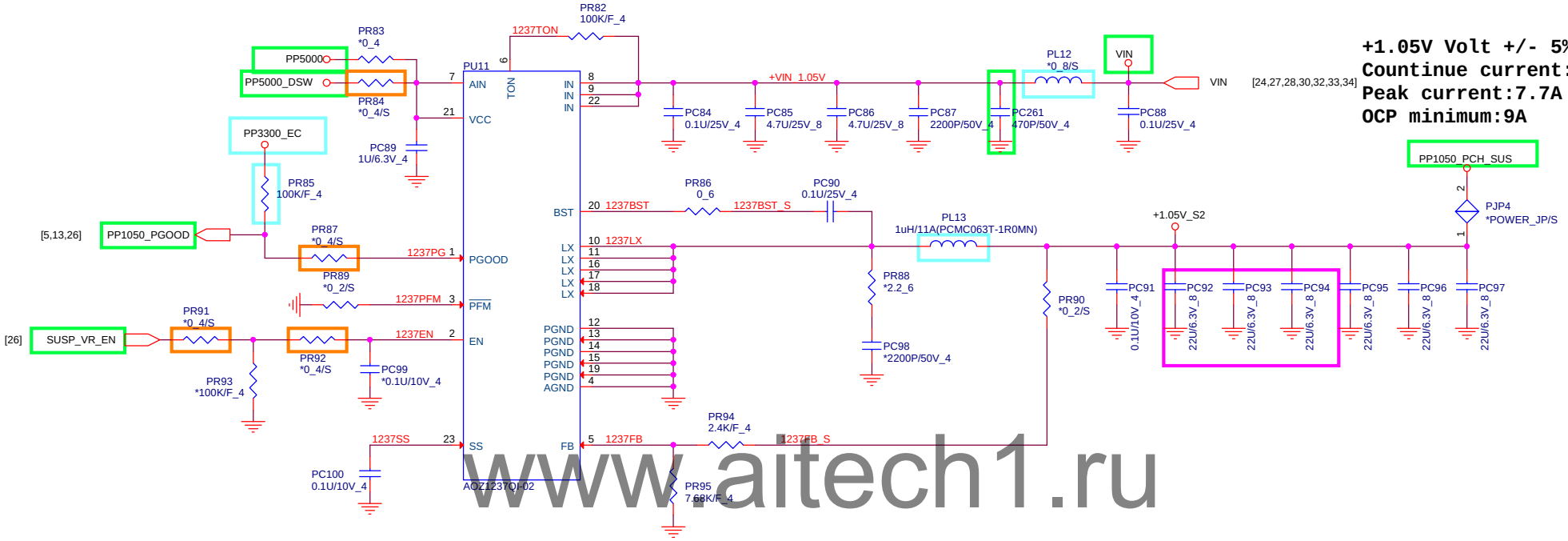
PROJECT : A23

| Size | Document Number | Rev. |
|---|---|---|
| Custom | DDR 1.35V(TPS51216) | 1A |
| Date: Friday, August 16, 2013 | Sheet : 30 of 42 | |

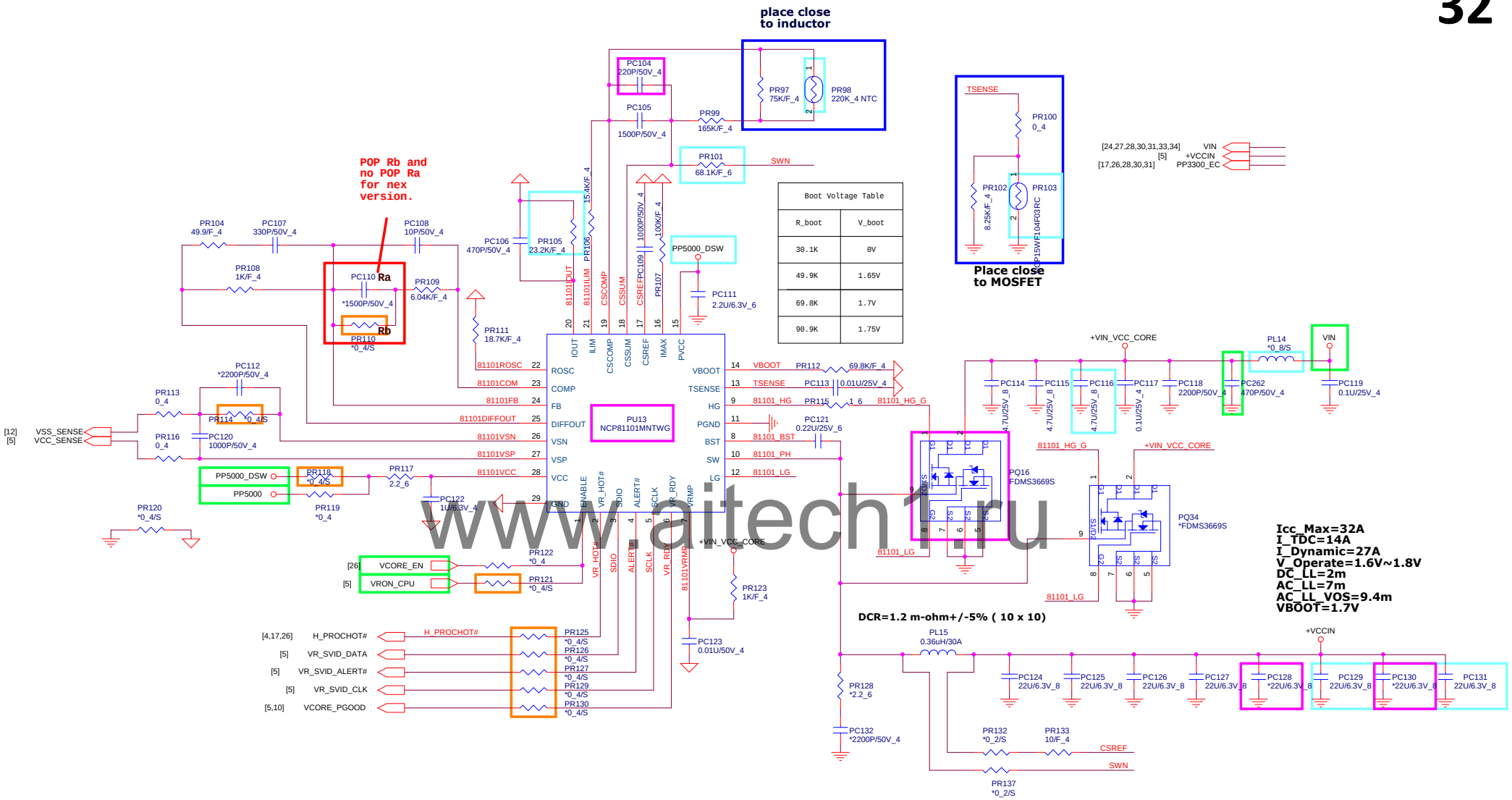





Quanta Computer Inc.

PROJECT : A23

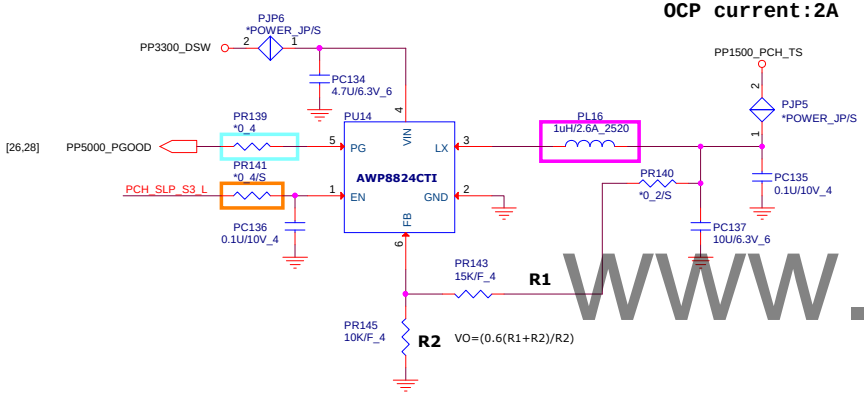
| Size | Document Number | Rev. |
|---|---|---|
| B | +1.05V(TPS51211) | 1A |
| Date: Friday, August 16, 2013 | Sheet : 31 of 42 | |

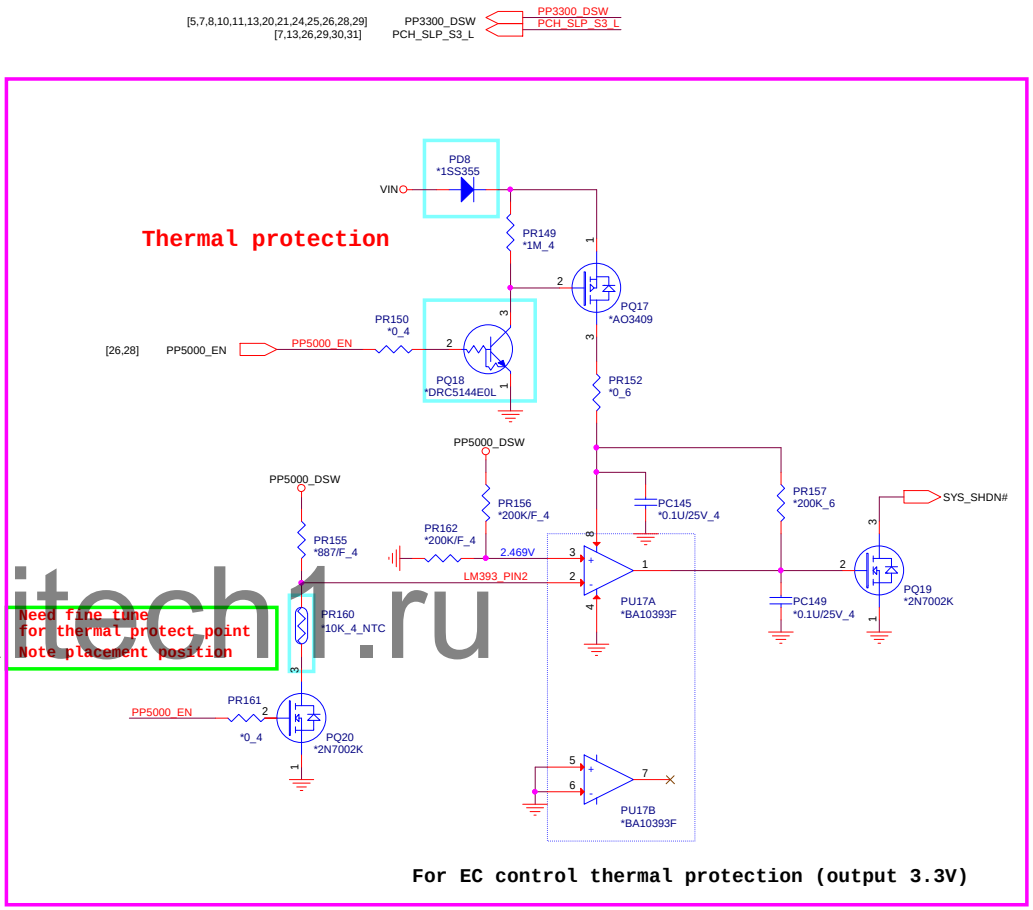





| | | | | |
|---|---|---|---|---|
| Quanta Computer Inc. | | | | |
| PROJECT : A23 | | | | |
| Size: Custom | Document Number: NCP81101MNTXG | | | Rev: 1A |
| Date: Friday, August 16, 2013 | | Sheet : 32 of 42 | | |

+1.5V +/- 5%
Countinue current:1.3A
Peak current:1.5A
OCP current:2A



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|---|---|---|
| Custom | +1.2V/+1.5V/+1.8V/Thermal protect | 1A |
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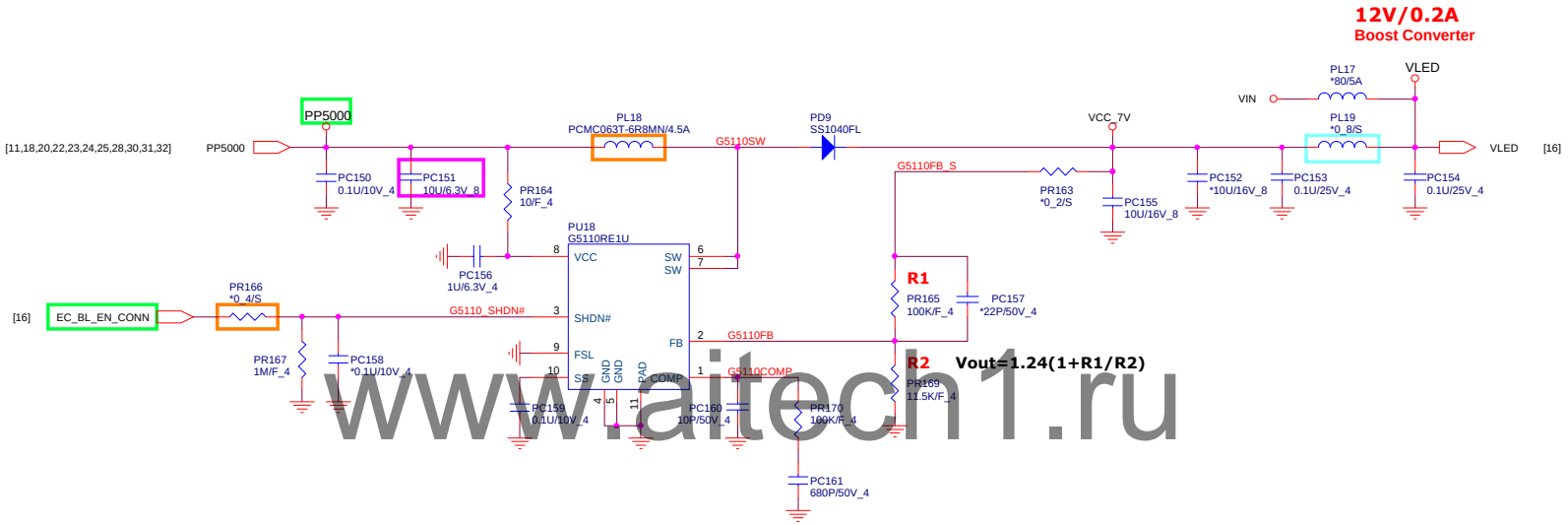




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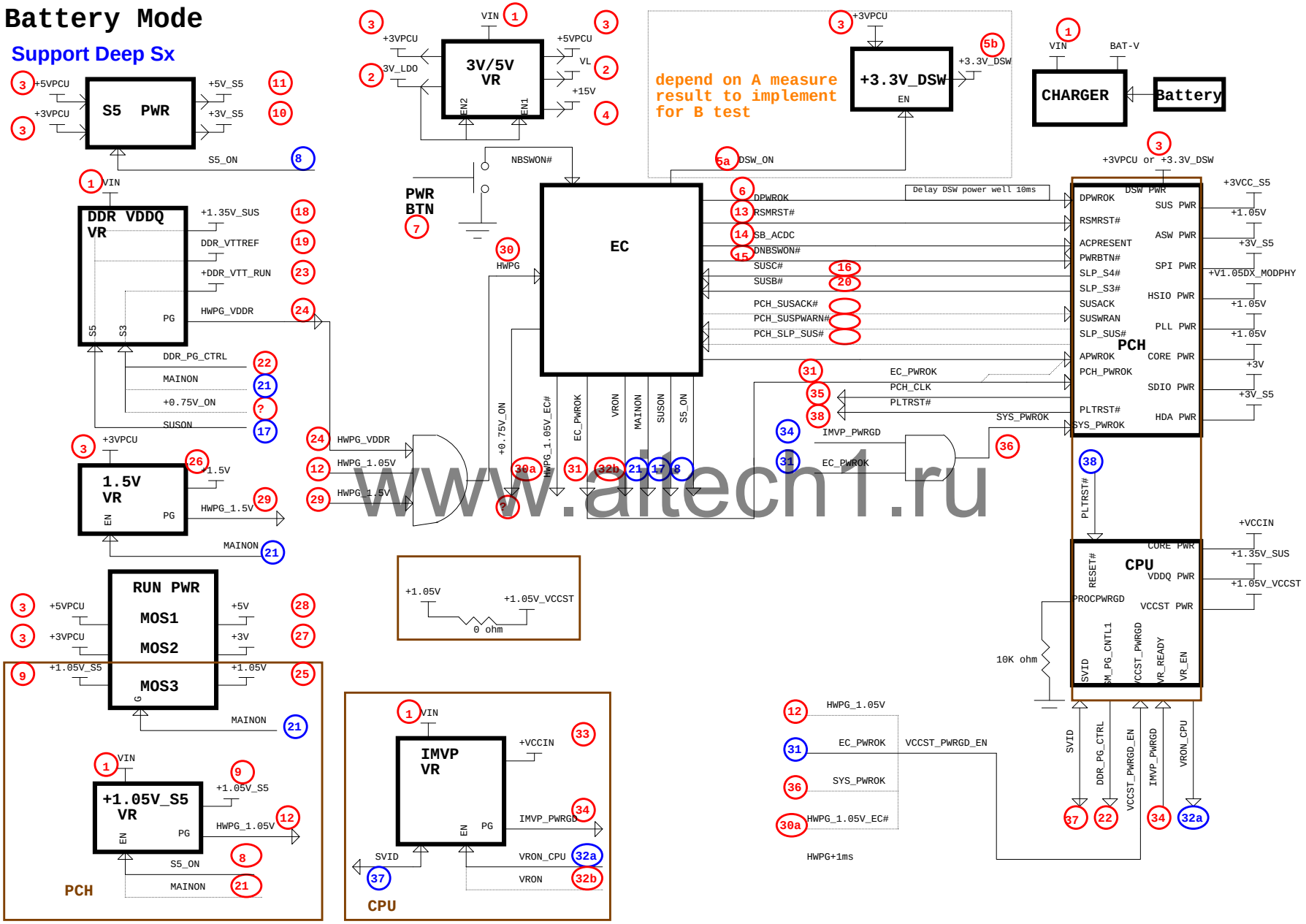
# Battery Mode

## Support Deep Sx



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| C | Power Sequence | 1A |
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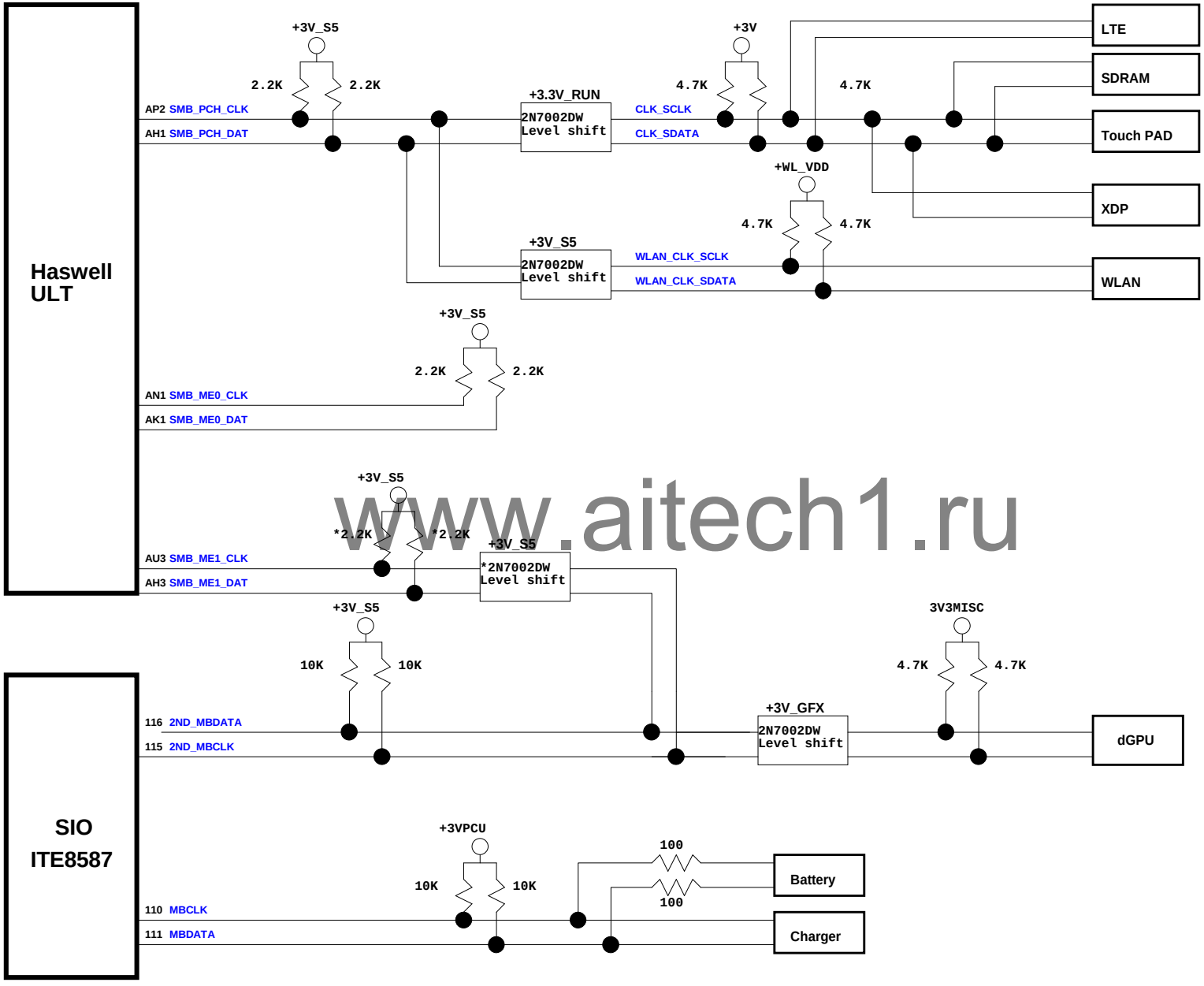




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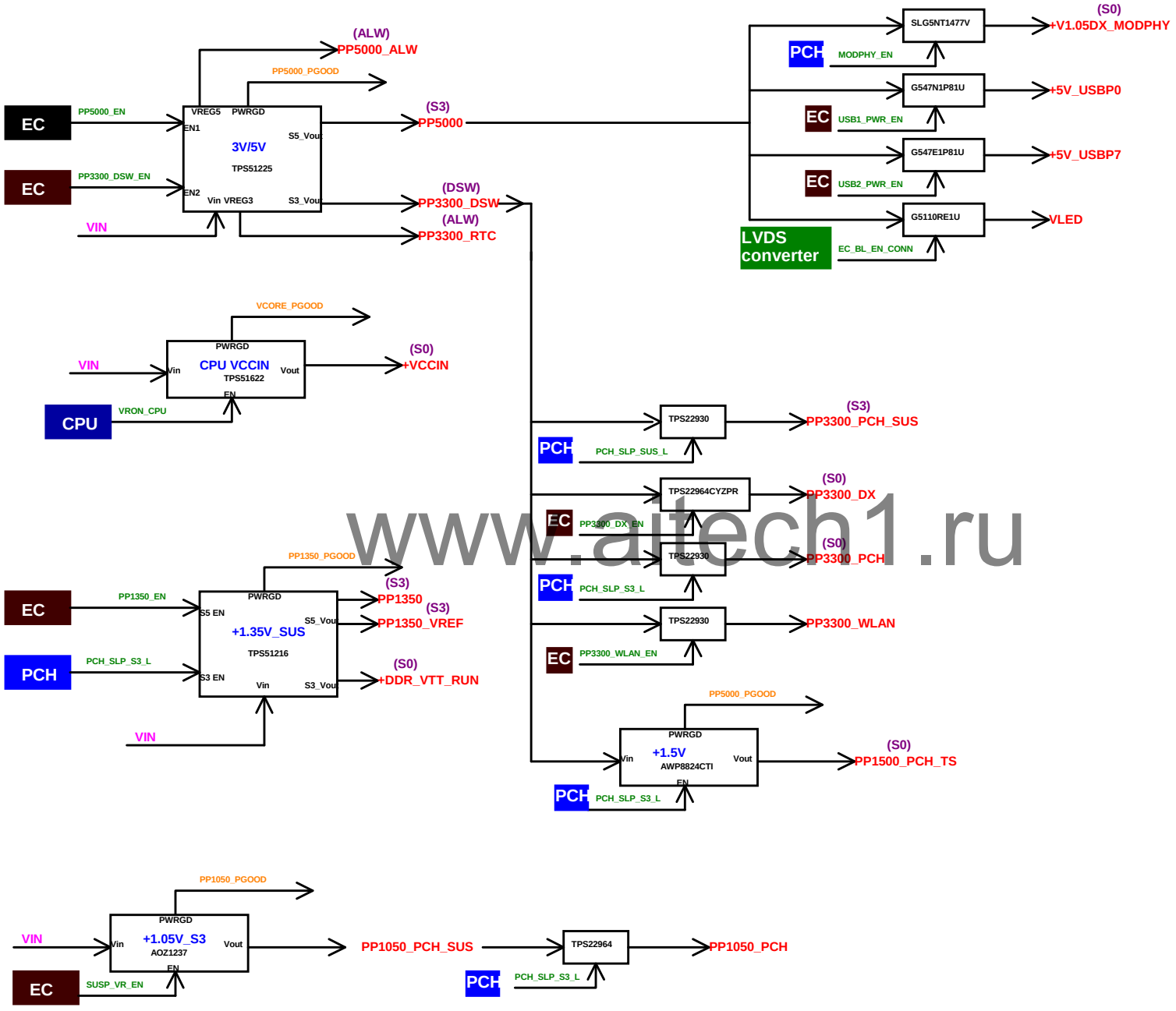




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| Model | Version | CHANGE LIST |
|---|---|---|
| | 1A | 1. CN4.18 connect to PP3300_EC. (5/3)<br>2. U27 change part number to SLG4K4137. (5/3)<br>3. Reserve Q67 , R6419 , R6418 and add bypass (R6516 and R6517). (5/3)<br>4. Stuff R266 and reserve R80. (5/3)<br>5. Reserve PP3300_DX power and PP3300_DSW power to pull up EC_FAN_TACH. (5/3)<br>6. Reserve Q64, R730, and R729, and use R6519 to bypass Fan PWM. (5/3)<br>7. Change USB2.0 port: MB_USB3.0_A → USBP0, MB_USB3.0_B → USBP1, and WWAN → USBP4. (5/3)<br>8. LED1 change PN to BEWH0046Z00. (5/6)<br>9. Add test point on SPI ROM for ICT. (5/6)<br>10. Modify EC_SMB0_DATA/CLK to EC_SMB2_DATA/CLK. (5/7)<br>11. Modify footprint of Hole6, Hole7, Hole8, and Hole9. (5/7)<br>12. Quantity of USB3.0 Power switch IC change from two to one. (5/7)<br>13. USB2.0 port: OC# → USB2_OC_L, Power enable → USB2_PWR_EN. (5/7)<br>14. Reserve EC_SMB1_CLK / EC_SMB1_DATA for LVDS converter debug. (5/7)<br>15. Stuff R6508 and reserve U6 because of LVDS power controling from RTD2132. (5/7)<br>16. Stuff R6498 because of Blacklight ON controling from RTD2132. (5/7)<br>17. Reserve U8 for LVDS converter debug. (5/7)<br>18. Remove R6414 (HDMI does not connect to LCDVCC). (5/7)<br>19. Remove D26 and PCBEEP_EC path. (5/7)<br>20. Stuff Q68, R280, and R279 for LVDS converter debug. (5/7)<br>21. Reserve PP1350_VREF to Vref_CA and Vref_DQ of DDR3L. (5/8)<br>22. R229 modity PN to CS31202FB15 (12K ohm +/-1%). (5/8)<br>23. C348 modity to 22uF (Realtek FAE recommend). (5/8)<br>24. Change PN and footprint of CN18 (MINIPCI Connector). (5/8)<br>25. Change PN of U28 (TPM IC). (5/8)<br>26. Change U5009 (thermal IC) to G708. (5/9)<br>27. KB_LED_EN connect to U5007.N12 (EC), and reserve 0 ohm. (5/9)<br>28. PWR_LED# connect to U5007.A6 (EC), and reserve 0 ohm. (5/9)<br>29. CN18 (MINIPCI CONN) add debug port signal. (5/9)<br>30. PP3300_EC add one 22uF cap. (5/9)<br>31. C259 change from 10uF to 22 uF. (5/9)<br>32. VIN add four 0.1uF/25V cap. (EC11, EC12, EC13, EC14). (5/9)<br>33. Audio +5V add one AZ2015-01H. (5/9)<br>34. Power circuit update. (5/9)<br>35. Audio codec confirm OK. (5/10)<br>36. Modify PN and footprint of connectors and key part IC byDick' confirmation. (5/10)<br>37. C782 change to 220uF_3528. (5/10)<br>38. SPI_WP_ME connect to CN27.13 (LVDS connector), and reserve 0 ohm. (5/10)<br>39. Modify footprint of Hole 2. (5/10)<br>40. Modify TP pin define. (5/10) |



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|---|---|---|
| | 1A | 41. Modify only one net from layout house. (5/10)<br>42. Remove Hole 16. (5/10)<br>43. Modify footprint of Hole 10 to be the same with Hole Hole8. (5/10)<br>44. Modify off page net by Michael. (5/10)<br>45. Modify pin define of Fan connector. (5/13)<br>46. Modify PN and footprint of connectors and key part IC byDick' confirmation. (5/13)<br>47. Modify footprint and PN of CN28 (NGFF SSD connector). (5/13)<br>48. C259 change from 22 uF to 10 uF, and C225 change from 10 uF to 22 uF. (5/13)<br>49. Remove Net: +3V_ADO, +1.5V, and +3VCC_S5. (5/13)<br>50. Remove RTC connector and its circuits. (5/13)<br>51. Remove off page Net: +3V_RTC, +V1.05S_APLLOPI, +V3.3DX_1.5DX_1.8DX_Audio. (5/13)<br>52. Modify pin define of CN4 (G-debug), follow 0C2. (5/13)<br>53. R6454 connect from +VCC_TS to PP3300_PCH_SUS. (5/13)<br>54. Q28.2 and R243 connect from PP3300_PCH_SUS to +VCC_TS. (5/13)<br>55. U5.3 connect to TP_SHDN_L (U5007.B8). (5/13)<br>56. Reserve R6469 and R6470 (USB interface of Touch screen). (5/13)<br>57. PWR_LED# connect to U5007.N11, and AD_TYPE connect to U5007.A6. (5/13)<br>58. Stuff R433 (SYS_SHD# connect to EC_EST#), and reserve PR46. (5/13)<br>59. KB_LED_EN connect to U5007.A4, BAT_LED0 connect to U5007.B2, and BAT_LED1 connect to U5007.B1. (5/13)<br>60. Swap pin3 and pin4 of Speaker connector. (5/13)<br>61. Update power circuit. (5/13)<br>62. Hole3 connect to ADOGND. (5/14)<br>63. Modify footprint of Hole7, Hole8, Hole9, and Hole10. (5/14)<br>64. Delete Hole6 and Hole14. (5/14)<br>65. Stuff R651, R598, and R649 for GPIO pull up resistor. (5/15)<br>66. Add R6536, R6537, R6538, R6539, R6540, R6541, R6542, and R6545 for GPIO pull up resistor. (5/15)<br>67. Un-stuff R679 for GPIO pull up resistor. (5/15)<br>68. Swap USBP6+ and USBP6- for layout. (5/15)<br>69. Add R6543 and R6544 for split J17 from R21 and T21 power plane. (5/15)<br>70. Power update. (5/15)<br>71. Add C5655 and C5654 for RF. (5/15)<br>72. R6472 change from 0805 type to 0603 type. (5/15)<br>73. Update power circuit. (5/16)<br>74. Delete un-used off page net. (5/16)<br>75. CN27.13 connect to GND, remove Write Protect. (5/16)<br>76. Reserve EC14, EC15, and EC16 to +VCCIN; EC17 to +WL_VDD; EC18 to +1.5V_MINI1_VDD; EC20, EC21, EC22, EC23, EC24, EC25, EC29, EC30, and EC31 to PP3300_DX; EC26, EC27, and EC28 to PP5000; EC32~EC40 to VIN for RF. (5/16)<br>77. Modify pin name of CN28.41, CN28.43, CN28.47, and CN28.49. (5/16)<br>78. Add three 10uF cap. and two 2.2uF cap. on VDDQ for Intel suggestion. (5/16)<br>79. Modify C88, C77, C89, and C79 from 47uF to 22uF for Intel suggestion. (5/16) |

| Model | Version | CHANGE LIST |
|---|---|---|
| | 1A (DB) | 80. Modify L33, L14, and L21 from 22uH to 0 ohm (R6546, R6547, and R6548) for Intel suggestion. (5/16)<br>81. Swap CN22.4 and CN22.6 for Intel suggestion. (5/16)<br>82. Add C5661~ C5665 for cross power plan cap. of VIN and PP3300_DSW. (5/16)<br>83. Un-stuff SW6 and R6511, and modify Hole5 to Write Protect function. (5/16)<br>84. R354 change from 100K ohm to 10K ohm, and reserve R6550 for Intel check list. (5/16)<br>85. CN28.69 connect to GND for SSD spec. (5/16)<br>86. C280 change to 1uF cap. and un-stuff C5650 for EC FAE suggestion. (5/16)<br>87. BAT_TEMP and D/C# add test point. (5/16)<br>88. R691 change from 120 ohm to 121 ohm for Intel suggestion. (5/17)<br>89. Remove EC16, EC22, EC23, EC25, EC26, EC32, EC38, EC39, C5663, and C5664 beacuse layout does not implement. (5/17)<br>90. Add R6551 and R6552 for I2C interface of touch screen. (5/17)<br>91. Change U27.6 from KB_COL02_SW to KB_COL03_SW, and Change U27.8 from KB_COL02 to KB_COL03. (5/17)<br>92. Reverse Pin define of Touch Pad. (5/17)<br>93. Add PAD1 and PAD2. (5/17)<br>94. Un-stuff C436, C434, C394, C703, C400, C374, and C438 for Intel suggestion. (5/17)<br>95. Modify R387 to 2.7 ohm, R345 to 5 ohm, and R474 to 5 ohm. (5/20)<br>96. Swap USB3 port 1 TX/RX signal for Layout. (5/20)<br>97. Reserve C5666 (0.1uF cap.) to GND on EC_FAN_TACH. (5/20)<br>98. Un-stuff R6494 and stuff R6495 for Intel suggestion. (5/20)<br>99. Un-stuff R428 and add R6553 (100k ohm) on U27.4. (5/20)<br>100. Power update. (5/20)<br>101. Add R6554 pull up to +1.05V_VCCST and 0.1 uF to GND. (5/20)<br>102. Stuff Intel XDP function. (5/23)<br>103. L1 and L5 change to 0 ohm. (5/23) |
| | 2A (SI) | 104. L1 and L5 change to 0 ohm (0603), and stuff R362. (6/11)<br>105. Remove SW6. (6/13)<br>106. Power of CN1 are selected between PP3300_DSW and PP3300_PCH_SUS. (6/13)<br>107. Add PP3300_DSW for touch screen power. (6/13)<br>108. Modify R6419 and R6418 pull up to +VCC_TS. (6/13)<br>109. Stuff Q67, R6419, and R6418, un-stuff R6516 and R6517. (6/13)<br>110. CN32.9 and CN32.52 connect to PP1050_PCH_SUS. (6/13)<br>111. Stuff C203, C204, and C205 for Power suggection. (6/13)<br>112. Modify footprint of CN24. (6/13)<br>113. Power update. (6/13)<br>114. Change R6455 to pull up to PP3300_DX, and U17.41/U17.46 connect to +5VA. (6/17)<br>115. Un-stuff L16, stuff U5008, C1012, C346, and C345, and add L57 on Audio IC. (6/17)<br>116. Change footprint and pin define of CN5. (6/17)<br>117. Change C307 to 22pF, C311 to 18pF, C624 to 12pF, and C625 to 12pF for Crystal cap. (6/17)<br>118. Power update. (6/17) |



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| | 2A (SI) | **119. Change C193 and C299 to 0.22uF for fix AC Insert issue. (6/18)**<br>**120. Un-stuff PC128 and C567 for layout mistake. (6/18)**<br>**121. Stuff R6489, U6, R6423, and C22, un-stuff R6498, R6507, and R6508 for LVDS control. (6/18)**<br>**122. R6489, R6438, and R6498 change to 1k ohm. (6/20)**<br>**Power change list:**<br>**123. Stuff PR47, PR85, PR75, PC116, PC128, PR240, PR256, PC129, PC130, and PC131, and un-stuff PR262, PR264, PQ32, and PR259. (6/20)**<br>**124. PU13 pin5 power source change from +5VS to PP5000_DSW. (6/20)**<br>**125. Delete PR139, PR244, and PR260. (6/20)**<br>**126. Change footprint of PJ1. (6/20)**<br>**127. PL6, PL7, PL10, PL12, PL14, PL19, PL20, PL22 change to 0 ohm. (6/20)**<br>**128. PL6, PL7, PL10, PL12, PL14, PL19, PL20, and PL22 change to short pad. (6/20)**<br>**129. PQ26 and PQ30 change from N-MOS to P-MOS. (6/20)**<br>**130. PC242 and PR247 Change from 100k_0402 to 4.7k_0402. (6/20)** |
| | 3A (PV) | **131. Un-stuff R478, R479, R477, and R480. (6/21)**<br>**132. Change Value of L32, L12, L13, L34, L19, and L15 to DLP11SA900HL2. (6/21)**<br>**133. Stuff U5, R6453, and R88, un-stuff R6452 and R89. (6/21)**<br>**134. Reverse PD38. (6/21)**<br>**135. Modify PR101 from 69.8k ohm to 68.1k ohm for Loadline, and PR105 from 23.7k ohm to 23.2k ohm for Iout. (6/24)**<br>**136. Add R6558, R6559, R6560, R6561, and R6562 for current leakage debug. (7/9)**<br>**137. Change R6489, R6438, and R6498 to 0 ohm, and add R6563 on BL_ON curcuit. (7/9)**<br>**138. Add PCH_RSMRST_L to connect to CN32.50. (7/9)**<br>**139. Add R6565 pull up to PP3300_DSW, and D49 on LID curcuit. (7/9)**<br>**140. Un-stuff CN11 and CN22. (7/9)**<br>**Power change list:**<br>**141. Change PN of PJ1 from DFHD11MS013 to DFHD11MS014. (7/12)**<br>**142. Rotate the direction of PD38. (7/12)**<br>**143. Un-stuff PD27, PD28, PC218, PC219, PC220, PC221, PR221, PR222 for BAT_LED control from P-MOS. (7/12)**<br>**144. PC151 change from CH6101KEA00 to CH61001KA94, PL11 change from CV+82D0MZ04 to CV+8213MZ00, PQ16 change from BAM03S30000 to BAM36690000, and stuff PC104. (7/12)**<br>**145. R204 change to PP3300_PCH, and un-stuff R225 and R6531 for power leakage. (7/12)**<br>**146. Change material and circuit of U5008. (7/15)**<br>**147. Remove KB Light circuit. (7/15)**<br>**148. Add U5010 and its circuit for TouchPad power. (7/15)**<br>**149. Un-stuff R717, and stuff R704. (7/15)**<br>**150. C299 connect to LID_OPEN. (7/15)**<br>**151. Add R6572 (100k ohm) for U5008 enable pin, and R6573/R6574 for LVDS PWM. (7/15)**<br>**152. Un-stuff all Touch screen circuit. (7/15)**<br>**153. Change PL16 from 2.2uH to 1.0uH, and modify footprint of PJ1. (7/15)** |



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| | 3A (PV) | **154. Change footprint of Hole4. (7/16)**<br>**155. Change R6565 pull up from PP3300_DSW to PP3300_EC. (7/16)**<br>**156. Change 0 ohm to short pad on R45,R69,R215,R236,R237,R274,R277,R288,R404,R513,R591,R639,R652,R653,R656,R596,R78,R86,R87,R6532,R173,R545,R587,R625 R641,R226,R265,R283,R295,R453,R425,R426,R432,R6421,R6430,R6440,R568,R582,R6400,R6403,R6404,R771,R773,R816,R6413. (7/17)**<br>**Power change list:**<br>**157. Change PN of PU13 from AL081101001 to AL081101000. (7/17)**<br>**158. Un-stuff PU4, PC50, and PC51 for reserve PP3300_RTC. (7/17)**<br>**159. Un-stuff PU17,PQ19,PQ20,PQ18,PQ17,PD8,PR160,PR156,PR162,PR157,PR155,PR149,PR152,PR150,PR161,PC145,PC149 for reserve Thermal protection. (7/17)**<br>**160. Change PL8 and PL9 from 1.5uH to 2.2uH. (7/17)**<br>**161. Change C345 from 22uF (0805) to 10uF (0603). (7/17)**<br>**162. Change CN4 from DFHS50FS025 to DFHS50FS056. (7/17)**<br>**163. Change C782 from 150uF to 220uF for USB3.0 port Voltage drop. (7/18)**<br>**164. Stuff C45,C46,C222,C207,L36,C273,C357,C639,EC33,EC37,EC40,EC34,EC36,EC35, and un-stuff R725,R724 for RF suggestion. (7/18)**<br>**165. Stuff L56,L32,L34, and un-stuff R494,R495,R493,R492,R6467,R6468 for EMI suggestion. (7/18)**<br>**Power change list:**<br>**166. Stuff EC3,EC5 for EMI suggestion, and stuff PC92,PC93,PC94 for RF suggestion. (7/18)**<br>**167. Change PJ1 from DFHD11MS014 to DFHD11MS013. (7/18)**<br>**168. Un-stuff PC128 and PC130 because height-limit . (7/18)**<br>**169. Change L12,L13,L15,L19,L32,L34,L36 from DC09004A014 to CX1HN900000. (7/19)**<br>**170. Stuff R717, and un-stuff R704 for Google suggestion. (7/23)** |
| | 3B (MV) | **171. Modify Net name of CN21.5. (8/13)**<br>**172. Add R6575 pull up to PP3300_DX. (8/13)**<br>**173. Stuff C5670. (8/13)**<br>**174. Reserve Q69, R6576, R6577, and R6578 for Audio codec FAE suggestion. (8/13)**<br>**175. R239,R353,R417,R433,R541,R546,R547,R548,R549,R552,R553,R570,R573,R6315,R6316,R6432,R6436,R6437R6519,R6558,R6559,R6560,R6561,R6562,R664,R719,R722, R757,R786,R813,L1,L38,L5,R107,R111,R158,R194,R197,R204,R212,R233,R234,R254,R337,R338,R373,R382,R411,R627,R6472,R6543R6544,R6556,R165,R170,R179,R190, R217,R270,R323,R559,R560,R6473,R6546,R6547,R6548,R732,R749 change from 0 ohm resistor to short pad. (8/13)**<br>**176. Modify M_A_A<9> connecting to R379, and M_A_A<3> connecting to R783. (8/14)**<br>**177. Modify M_A_DIM0_CK_DDR0_DP connecting to R769, and M_A_DIM0_CK_DDR0_DN connecting to R755. (8/14)**<br>**178. Footprint of Hole5 change to H-TC315BE315X315D106NP2. (8/15)**<br>**Power change list:**<br>**179. PR70,PR77,PR73,PR81,PR48,PR44,PR171,PR173,PR174,PR175,PR265,PR87,PR92,PR84,PR91,PR118,PR121,PR125,PR126,PR127,PR129,PR130,PR110,PR114,PR166,PR141 change from 0 ohm resistor to short pad. (8/15)**<br>**180. PL18 change from CV-6825MZ00 to CV-6845MZ05 for change to common part. (8/15)**<br>**181. Un-staff CN4, and Hole13 change to floating. (8/16)**<br>**182. Remove R725,R724,R6467,R6468,L27,L29,R493,R492,L12,L13,R494,R495,L19,L15 for canceling colay of USB port. (8/16)**<br>**183. R99,R100,R101,R102,R56,R59,R60,R61,R65,R66,R544,R6521,R6495,R88,R90,R266 change from 0 ohm resitstor to short pad. (8/16)** |